Chapter 27

Electronics

Semiconductor electronics

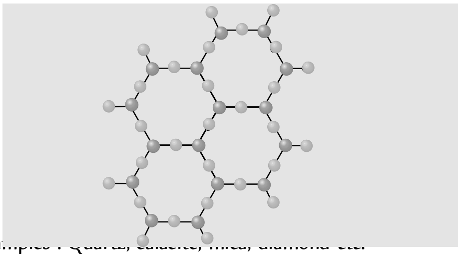
Solids

It is a state of matter which has a definite shape and a definite volume. The characteristic properties of the solid depends upon the nature of forces acting between their constituent particles (*i.e.* ions, atoms or molecules). Solids are divided into two categories.

Crystalline solids

(1) These solids have definite external geometrical form.

(2) Ions, atoms or molecules of these solid are arranged in a definite fashion in all it's three dimensions.



(3) Examples : Quartz, calcite, mica, diamond etc.

(4) They have well defined facets or faces.

(5) They are ordered at short range as well as at long range.

(6) They are anisotropic, *i.e.* the physical properties like elastic modulii, thermal conductivity, electrical conductivity, refractive index have different values in different direction.

(7) They have sharp melting point.

(8) Bond strengths are identical throughout the solid.

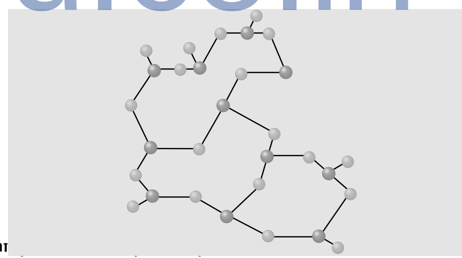
(9) These are considered as true solids.

(10) An important property of crystals is their symmetry.

Amorphous or glassy solids

(1) These solids have no definite external geometrical form.

(2) Ions, atoms or molecules of these solids are not arranged in a definite fashion.



(3) Exa

(4) They do not possess definite facets or faces.

(5) These have short range order, and there is no long range order.

(6) They are isotropic.

(7) They do not have a sharp melting point.

(8) Bond strengths vary.

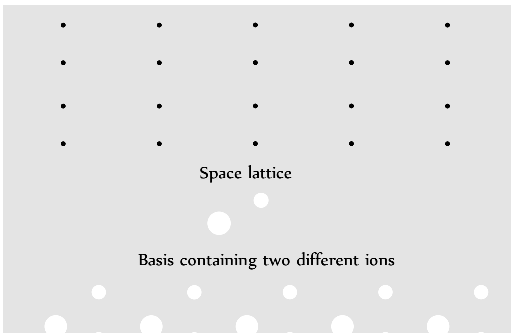
(9) These are considered as pseudo-solids or super cooled liquids.

(10) Amorphous solids do not have any symmetry.

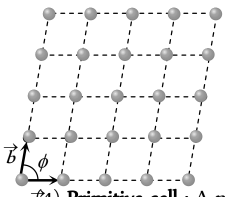
Terms Related with Crystal Structure

(1) **Crystal lattice :** It is a geometrical arrangement of points in space where if atoms or molecules of a solid are placed, we obtain an actual crystal structure of the solid.

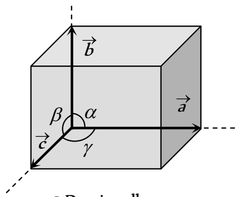
(2) **Basis :** The atoms or molecules attached with every lattice point in a crystal structure is called the basis of crystal structure.



(3) **Unit cell :** Is defined as that volume of the solid from which the entire crystal structure can be constructed by the translational repetition in three dimensions. The length of three sides of a unit cell ($3D$) are called primitives or lattice constant they are denoted by *a, b, c*



2D unit cell



3D unit cell

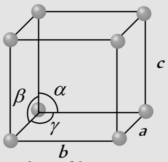
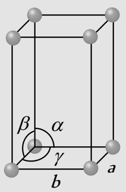
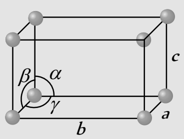
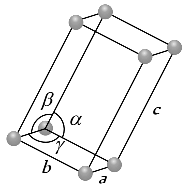
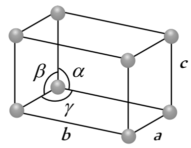
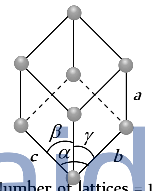
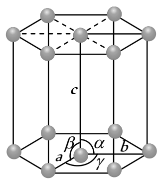
Fig. 27.1

(4) **Primitive cell :** A primitive cell is a minimum volume unit cell or the simple unit cell with particles only at the corners is a primitive unit cell and other types of unit cells are called non-primitive unit cells. There is only one lattice point per primitive cell.

(5) **Crystallographic axis :** The lines drawn parallel to the lines of intersection of the faces of the unit cell are called crystallographic axis.

All the crystals on the basis of the shape of their unit cells, have been divided into seven crystal systems as shown in the following table.

Table 27.1 : Different crystal systems

System	Lattice constants	Angle between lattice constants	Examples
Cubic  Number of lattices = 3	$a = b = c$	$\alpha = \beta = \gamma = 90°$	Diamond, $NaCl$, Li, Ag, Cu, NH_4Cl, Pb *etc.*
Tetragonal  Number of lattices = 2	$a = b \neq c$	$\alpha = \beta = \gamma = 90°$	White tin, $NiSO_4$ *etc.*
Orthorhombic  Number of lattices = 4	$a \neq b \neq c$	$\alpha = \beta = \gamma = 90°$	$HgCl_2$, KNO_3, gallium *etc.*
Monoclinic  Number of lattices = 2	$a \neq b \neq c$	$\alpha = \gamma = 90°$ and $\beta \neq 90°$	$KClO_3$, $FeSO_4$ *etc.*
Triclinic  Number of lattices = 1	$a \neq b \neq c$	$\alpha \neq \beta \neq \gamma \neq 90°$	$K_2Cr_2O_7$, $CuSO_4$ *etc.*
Rhombo-hedral or Trigonal  Number of lattices = 1	$a = b = c$	$\alpha = \beta = \gamma \neq 90°$	Calcite, *As, Sb, Bi etc.*
Hexagonal  Number of lattices = 1	$a = b \neq c$	$\alpha = \beta = 90°$ and $\gamma = 120°$	*Zn, Cd, Ni etc.*

Different Types of Symmetry in Cubic Lattices

(1) **Centre of symmetry :** An imaginary point within the crystal such that any line drawn through it intersects the surface of the crystal at equal distances in both directions.

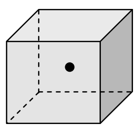
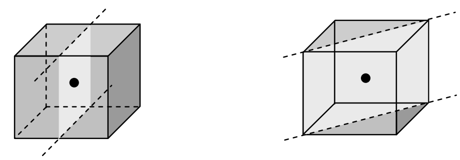


Fig. 27.2

(2) **Plane of symmetry :** It is an imaginary plane which passes through the centre of a crystal and divides it into two equal portions such that one part is exactly the mirror image of the other.



(A) Rectangular plane of symmetry

(B) Diagonal plane of symmetry

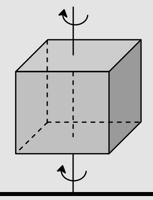
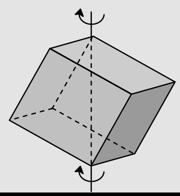
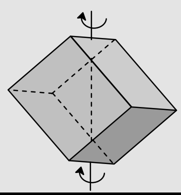
Fig. 27.3

A cubical crystal possesses six diagonal plane of symmetry and three rectangular plane of symmetry.

(3) **Axis of symmetry** : It is an imaginary straight line about which, if the crystal is rotated, it will present the same appearance more than once during the complete revolution.

In general, if the same appearance of a crystal is repeated on rotating through an angle $\frac{360^o}{n}$, around an imaginary axis, the axis is called an *n*-fold axis.

Table 27.2 : A cubical crystal possesses in all 13 axis of symmetry

Axis of four-fold symmetry = 3 (Because of six faces)	Axis of three-fold symmetry = 4 (Because of eight corners)	Axis of two-fold symmetry = 6 (Because of twelve edges)
		

(4) **Elements of symmetry** : The total number of planes, axes and centre of symmetry possessed by a crystal are termed as elements of symmetry. A cubic crystal possesses a total of 23 elements of symmetry.

Planes of symmetry $= (3+6) = 9$,

Axes of symmetry $= (3+4+6) = 13$,

Centre of symmetry = 1.

Total number of symmetry elements = 23

More About Cubic Crystals

(1) **Different lattice in cubic crystals** : There are three lattice in the cubic system.

(i) The simple cubic (*sc*) lattice.

(ii) The body-centered cubic (*bcc*).

(iii) The face-centered cubic (*fcc*).

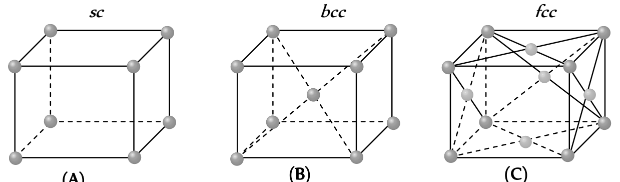


Fig. 27.4

(2) **Atomic radius** : The half of the distance between two atoms in contact is defined as atomic radius.

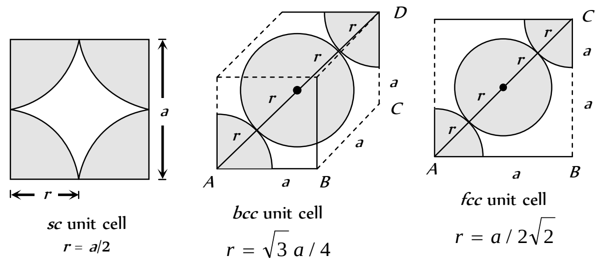


Fig. 27.5

(3) **Atoms per unit cell** : An atom located at the corner of a unit cell of a lattice is shared equally by eight other unit cells in the three dimensional lattice. Therefore, each unit cell has 1/8 share of an atom at its each corner. Similarly, a face of the unit cell is common to the two unit cells in the lattice. Therefore, each unit cell has 1/2 share of an atom at its each face. The atom located at the centre of the unit cell belongs completely to the unit cell.

Let N_c, N_b and N_f be the number of atoms at the corners, centre and face of the unit cell respectively. Therefore the number of atoms per unit cell is given by $N = N_b + \frac{N_f}{2} + \frac{N_c}{8}$

(i) In *sc* lattice : $N_b = 0,\ N_f = 0,\ N_c = 8$ so $N = 1$

(ii) In *bcc* lattice : $N_b = 1,\ N_f = 0,\ N_c = 8$ so $N = 2$

(iii) In *fcc* lattice : $N_b = 0,\ N_f = 6,\ N_c = 8$ so $N = 4$

(4) **Co-ordination number** : It is defined as the number of nearest neighbours that an atom has in a unit cell. It depends upon structure.

(i) Simple cubic structure : Each atom has two neighbours along *X*-axis, two along *Y*-axis and two along *Z*-axis so co-ordination number = 6.

(ii) Face-centred cubic structure: Every corner atom has four neighbours in each of the three planes *XY*, *YZ*, and *ZX* so co-ordination number = 12

(iii) Body-centred cubic structure: The atom of the body of the cell has eight neighbours at eight corner of the unit cell so co-ordination number = 8.

(5) **Atomic packing fraction (or packing factor or relative packing density)**

The atomic packing fraction indicates how close the atoms are packed together in the given crystal structure or the ratio of the volume occupied by atoms in a unit cell in a crystal and the volume of unit cell is defined as APF.

(i) **For *sc* crystal** : Volume occupied by the atom in the unit cell $= \frac{4}{3}\pi r^3 = \frac{\pi a^3}{6}$. Volume of the unit cell $= a^3$

Thus P.F. $= \frac{\pi a^3/6}{a^3} = \frac{\pi}{6} = 0.52 = 52\%$

(ii) **For *bcc*** : P.F. $= \frac{\sqrt{3}\pi}{8} = 68\%$

(iii) **For *fcc*** : P.F. $= \frac{\pi}{3\sqrt{2}} = 74\%$

(6) **Density of unit cell** : Density of unit cell $= \frac{\text{Mass of the unit cell}}{\text{Volume of the unit cell}} = \frac{nA}{NV} = \frac{nA}{Na^3}$

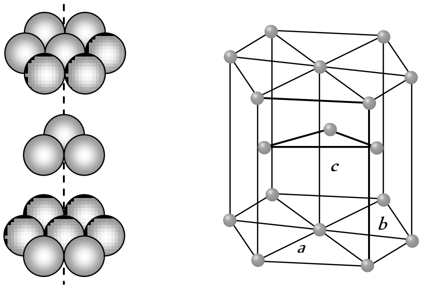
where *n* = Number of atoms in unit cell (For *sc* lattice *n* = 1, for *bcc* lattice *n* = 2, for *fcc* lattice *n* = 4), *A* = atomic weight, *N* = Avogadro's number, *V* = Volume of the unit cell.

(7) **Bond length** : The distance between two nearest atoms in a unit cell of a crystal is defined as bond length.

(i) In a *sc* lattice : Bond length = *a* (ii) In a *bcc* lattice : Bond length $= \frac{\sqrt{3}a}{2}$ (iii) In a *fcc* lattice : Bond length $= \frac{a}{\sqrt{2}}$

Hexagonal Close Packed (HCP) Structure

The HCP structure also maximizes the packing fraction



(A) Fig. 27.6 (B)

(1) $a = b \neq c$

(2) Number of atoms per unit cell = 6

(3) The volume of the hexagonal cell = $3\sqrt{2}\,a^3$

(4) The packing fraction $= \dfrac{\pi\sqrt{2}}{6}$

(5) Coordination number = 12

(6) Magnesium is a special example of HCP lattice structure.

Bonding Forces in Crystals

The properties of a solid are mainly determined by the type of bonding that exists between the atoms. According to bonding in crystals they are classified into following types.

(1) **Ionic crystal :** This type of bonding is formed due to transfer of electrons between atoms and consequent attraction between them.

(i) In *NaCl* crystal, the electron of *Na* atom is transferred to chlorine atom. In this way *Na* atom changes in to *Na* ion and *Cl* atom changes into *Cl* ion.

(ii) Cause of binding is electrostatic force between positive and negative ion.

(iii) These crystal are usually hard, brittle and possesses high melting and boiling point.

(iv) These are bad conductor of electricity.

(v) Common example are *NaCl, CsCl, LiF etc.*

(2) **Covalent crystal :** Covalent bonding is formed by sharing of electrons of opposite spins between two atoms

(i) The conductivity of these solids rise with rise in temperature.

(ii) These crystal posses high melting point.

(iii) Bonding between H_2, Cl_2 molecules *Ge, Si*, Quartz, diamond *etc.* are common example of covalent bonding

(3) **Metallic bonds :** This type of bonding is formed due to attraction of valence (free) electrons with the positive ion cores

(i) Their conductivity decreases with rise of temperature.

(ii) When visible light falls on a metallic crystal, the electrons of atom absorb visible light, so they are opaque to visible light. However some orbital electrons absorb energy and reach in excited state. They then return to their normal states, remitting light of same frequency.

Common examples are *Na, Li, K, Cs, Au, Hg etc.*

(4) **Vander waal's crystal :** These crystal consists of neutral atoms or molecules bonded together in solid phase by weak, short range attractive forces called vander Waal's forces.

(i) This bonding is weakest and occurs in solid CO_2, methane, paraffin, ice, etc.

(ii) They are normally insulator, they are soft, easily compressible and posses low melting point.

(5) **Hydrogen bonding :** Hydrogen bonding is due to permanent dipole interaction.

(i) This bond is stronger than vander Waal's bond but much weaker than ionic and covalent bond.

(ii) They possesses low melting point.

(iii) Common examples are H_2O, *HF etc.*

Single, Poly and Liquid Crystals

(1) **Single crystal :** The crystals in which the periodicity of the pattern extends throughout the piece of the crystal are known as single crystals. Single crystals have anisotropic behaviour *i.e.* their physical properties (like mechanical strength, refractive index, thermal and electrical conductivity) are different along different directions. The small sized single crystals are called mono-crystals.

(2) **Poly-crystals :** A poly-crystal is the aggregate of the monocrystals whose well developed faces are joined together so that it has isotropic properties. Ceramics are the important illustrations of the poly-crystalline solids.

(3) **Liquid crystals :** The organic crystalline solid which on heating, to a certain temperature range becomes fluid like but its molecules remain oriented in a particular directions, showing that they retain their anisotropic properties, is called liquid crystal. These crystals are used in a liquid crystal displays (L.C.D.) which are commonly used in electronic watches, clocks and micro-calculators *etc.*

Energy Bands

This theory is based on the Pauli exclusion principle.

In isolated atom the valence electrons can exist only in one of the allowed orbitals each of a sharply defined energy called energy levels. But when two atoms are brought nearer to each other, there are alterations in energy levels and they spread in the form of bands.

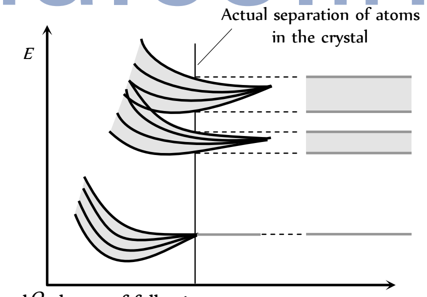


Fig. 27.7 Origin of energy bands in a solid

Energy bands are of following types

(1) **Valence band :** The energy band formed by a series of energy levels containing valence electrons is known as valence band. At 0 *K*, the electrons fills the energy levels in valence band starting from lowest one.

(i) This band is always filled with electrons.

(ii) This is the band of maximum energy.

(iii) Electrons are not capable of gaining energy from external electric field.

(iv) No flow of current due to electrons present in this band.

(v) The highest energy level which can be occupied by an electron in valence band at 0 *K* is called fermi level.

(2) **Conduction band :** The higher energy level band is called the conduction band.

(i) It is also called empty band of minimum energy.

(ii) This band is partially filled by the electrons.

(iii) In this band the electrons can gain energy from external electric field.

(iv) The electrons in the conduction band are called the free electrons. They are able to move any where within the volume of the solid.

(v) Current flows due to such electrons.

(3) **Forbidden energy gap (ΔE) :** Energy gap between conduction band and valence band $\Delta E_g = (C.B.)_{min} - (V.B.)_{max}$

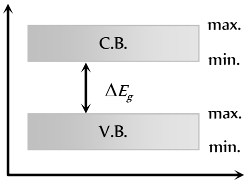


Fig. 27.8

(i) No free electron is present in forbidden energy gap.

(ii) Width of forbidden energy gap depends upon the nature of substance.

(iii) As temperature increases (↑), forbidden energy gap decreases (↓) very slightly.

Table 27.3 : Types of solid

Properties	Conductors	Insulators	Semiconductors
Electrical conductivity	10^2 to 10^8 ℧$/m$	10^{-8} ℧$/m$	10^{-5} to 10^0 ℧$/m$
Resistivity	10^{-2} to 10^{-8} Ω-m (negligible)	10^8 Ω-m	10^5 to 10^0 Ω-m
Band structure	C.B. V.B.	C.B. ΔE_g (large) V.B.	C.B. ΔE_g (small) V.B.
Energy gap (E_g)	Zero or very small	Very large; for diamond it is 6 *eV*	$Ge \rightarrow 0.7$ *eV* $Si \rightarrow 1.1$ *eV* $GaAs \rightarrow 1.3$ *eV* $GaF_2 \rightarrow 2.8$ *eV*
Current carriers	Free electrons	—	Free electrons and holes
Condition of V.B. and C.B. at ordinary temperature	V.B. and C.B. are completely filled or C.B. is some what empty	V.B. – completely filled C.B. – completely unfilled	V.B. – somewhat empty C.B. – somewhat filled
Temperature co-efficient of resistance	Positive	Zero	Negative
Effect of temperature on conductivity	Decreases	—	Increases
Effect of temperature on resistance	Increases	—	Decreases
Examples	*Cu, Ag, Au, Na, Pt, Hg* etc.	Wood, plastic, mica, diamond, glass etc.	*Ge, Si, Ga, As* etc.
Electron density	$10^{29}/m^3$	—	$Ge \sim 10^{19}\ /m^3$ $Si \sim 10^{16}\ /m^3$

Holes in Semiconductors

(1) When an electron is removed from a covalent bond, it leaves a vacancy behind. An electron from a neighbouring atom can move into this vacancy, leaving the neighbour with a vacancy. In this way the vacancy formed is called hole (or cotter), and can travel through the material and serve as an additional current carriers.

(2) A hole is considered as a seat of positive charge, having magnitude of charge equal to that of an electron.

(3) Holes acts as virtual charge, although there is no physical charge on it.

(4) Effective mass of hole is more than electron.

(5) Mobility of hole is less than electron.

Intrinsic Semiconductors

(1) A pure semiconductor is called intrinsic semiconductor. It has thermally generated current carriers

(2) They have four electrons in the outermost orbit of atom and atoms are held together by covalent bond

(3) Free electrons and holes both are charge carriers and n_e (in C.B.) $= n_h$ (in V.B.)

(4) The drift velocity of electrons (v_e) is greater than that of holes (v_h)

(5) For them fermi energy level lies at the centre of the C.B. and V.B.

(6) In pure semiconductor, impurity must be less than 1 in 10^8 parts of semiconductor.

(7) In intrinsic semiconductor

$n_e^{(o)} = n_h^{(o)} = n_i$; where $n_e^{(o)}$ = Electron density in conduction band, $n_h^{(o)}$ = Hole density in V.B., n_i = Density of intrinsic carriers.

(8) The fraction of electrons of valance band present in conduction band is given by $f \propto e^{-E_g/kT}$; where E_g = Fermi energy or k = Boltzmann's constant and T = Absolute temperature

(9) Because of less number of charge carriers at room temperature, intrinsic semiconductors have low conductivity so they have no practical use.

(10) Number of electrons reaching from valence band to conduction band $n = AT^{3/2}e^{-E_g/2kT}$

Extrinsic Semiconductor

(1) An impure semiconductor is called extrinsic semiconductor

(2) When pure semiconductor material is mixed with small amounts of certain specific impurities with valency different from that of the parent material, the number of mobile electrons/holes drastically changes. The process of addition of impurity is called doping.

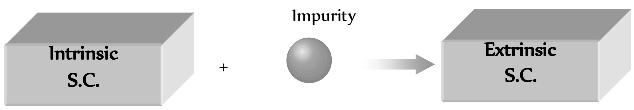


Fig. 27.9

(3) **Pentavalent impurities :** The elements whose atom has five valance electrons are called pentavalent impurities e.g. *As, P, Sb etc.* These impurities are also called donor impurities because they donate extra free electron.

(4) **Trivalent impurities :** The elements whose each atom has three valance electrons are called trivalent impurities e.g. *In, Ga, Al, B, etc.* These impurities are also called acceptor impurities as they accept electron.

(5) The compounds of trivalent and pentavalent elements also behaves like semiconductors *e.g. GaAs, InSb, In P, GaP etc.*

(6) The number of atoms of impurity element is about 1 in 10^8 atoms of the semiconductor.

(7) In extrinsic semiconductors $n_e \neq n_h$

(8) In extrinsic semiconductors fermi level shifts towards valence or conduction energy bands.

(9) Their conductivity is high and they are used for practical purposes.

(10) In a doped extrinsic semiconductor, the number density of e^- of the conduction band (n) and the number density of holes in the valence band (n) differs from that in a pure semiconductor. If n is the number density of electron in conduction band or the number density of holes in valence band in a pure semiconductor then $n_e n_h = n_i^2$ (mass action law)

(11) Extrinsic semiconductors are of two types

(i) *N*-type semiconductor (ii) *P*-type semiconductor

N-Type Semiconductor

These are obtained by adding a small amount of pentavalent impurity to a pure sample of semiconductor (*Ge*).

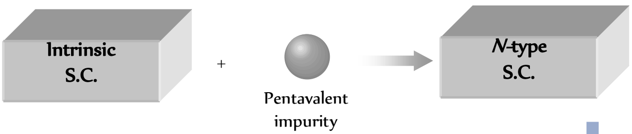


Fig. 27.10

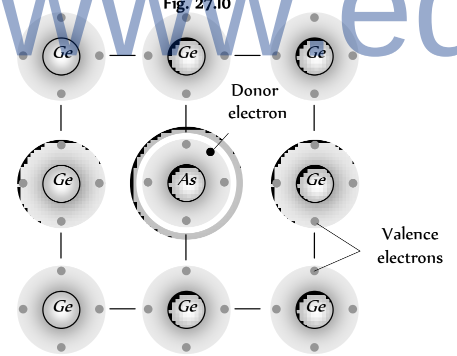


Fig. 27.11

(1) Majority charge carriers – electrons

Minority charge carriers – holes

(2) $n_e >> n_h$; $i_e >> i_h$

(3) Conductivity $\sigma \approx n_e \mu_e e$

(4) *N*-type semiconductor is electrically neutral (not negatively charged)

(5) Impurity is called Donar impurity because one impurity atom generate one electron.

(6) Donor energy level lies just below the conduction band.

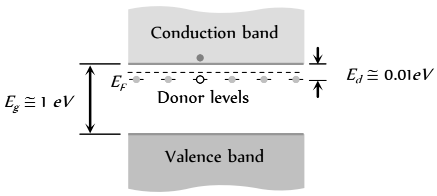
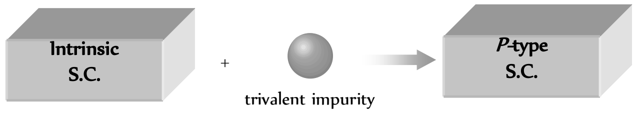


Fig. 27.12

P-Type Semiconductor

These are obtained by adding a small amount of trivalent impurity to a pure sample of semiconductor (*Ge*).



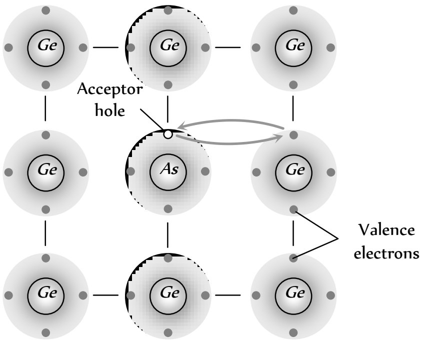


Fig. 27.13

(1) Majority charge carriers – holes

Minority charge carriers – electrons

(2) $n_h >> n_e$; $i_h >> i_e$

(3) Conductivity $\sigma \approx n_h \mu_h e$

(4) *P*-type semiconductor is also electrically neutral (not positively charged)

(5) Impurity is called Acceptor impurity.

(6) Acceptor energy level lies just above the valence band.

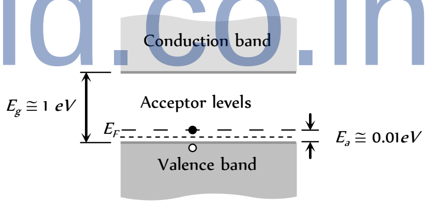


Fig. 27.14

Density of Charge Carriers

Due to thermal collisions, an electron can take up or release energy. Thus, occasionally a valence electron takes up energy and the bond is broken. The electron goes to the conduction band and a hole is created. And occasionally, an electron from the conduction band loses some energy, comes to the valence band and fills up a hole. Thus, new electron-hole pairs are formed as well as old electron-hole disappear. A steady-state situation is reached and the number of electron-hole pairs takes a nearly constant value. For silicon at room temperature (300 *K*), the number of these pairs is about 7×10^{15} *m*. For germanium, this number is about 6×10^{19} /*m*.

Table 27. 4 : Densities of charge carriers

Material	Type	Density of conduction electrons (m^{-3})	Density of holes (m^{-3})
Copper	Conductor	9×10^{28}	0
Silicon	Intrinsic semiconductor	7×10^{15}	7×10^{15}
Silicon doped with phosphorus (1 part in 10^6)	*N*-type semiconductor	5×10^{22}	1 $\times 10^9$

Silicon doped with aluminium (1 part in 10^6	*P*-type semiconductor	1×10^9	5×10^{22}

Conductivity of Semiconductor

(1) In intrinsic semiconductors $n_e = n_h$. Both electron and holes contributes in current conduction.

(2) When some potential difference is applied across a piece of intrinsic semiconductor current flows in it due to both electron and holes *i.e.* $i = i_e + i_h \Rightarrow i = eA[n_e v_e + n_h v_h]$

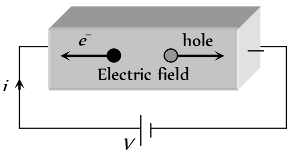


Fig. 27.15

(3) As we know $\sigma = \frac{J}{E} = \frac{i}{AE}$. Hence conductivity of semiconductor

$\sigma = e[n_e \mu_e + n_h \mu_h]$; where v_e = drift velocity of electron, v_h = drift velocity of holes, E = Applied electric field $\mu_e = \frac{v_e}{E}$ = mobility of electron and $\mu_h = \frac{v_h}{E}$ = mobility of holes

(4) Motion of electrons in the conduction band and of holes the valence band under the action of electric field is shown below

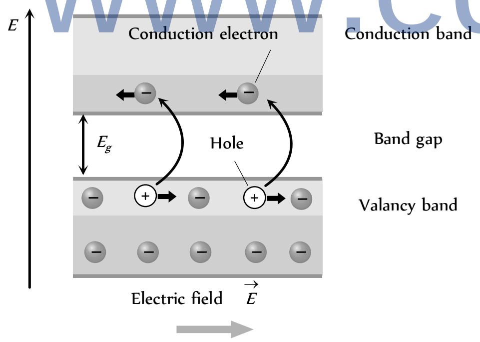


Fig. 27.16

(5) At absolute zero temperature (0 *K*) conduction band of semiconductor is completely empty *i.e.* σ = 0. Hence the semiconductor behaves as an insulator.

P-N Junction Diode

When a *P*-type semiconductor is suitably joined to an *N*-type semiconductor, then resulting arrangement is called *P-N* junction or *P-N* junction diode

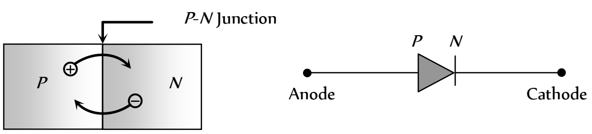


Fig. 27.17

(1) **Depletion region :** On account of difference in concentration of charge carrier in the two sections of *P-N* junction, the electrons from *N*-region diffuse through the junction into *P*-region and the hole from *P* region diffuse into *N*-region.

Due to diffusion, neutrality of both *N* and *P*-type semiconductor is disturbed, a layer of negative charged ions appear near the junction in the *P*-crystal and a layer of positive ions appears near the junction in *N*-crystal. This layer is called depletion layer

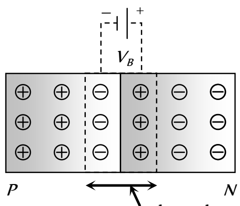


Fig. 27.18

(i) The thickness of depletion layer is 1 *micron* = 10^{-6} *m*.

(ii) Width of depletion layer $\propto \frac{1}{\text{Dopping}}$

(iii) Depletion is directly proportional to temperature.

(iv) The *P-N* junction diode is equivalent to capacitor in which the depletion layer acts as a dielectric.

(2) **Potential barrier :** The potential difference created across the *P-N* junction due to the diffusion of electron and holes is called potential barrier.

For *Ge* $V_B = 0.3V$ and for silicon $V_B = 0.7V$

On the average the potential barrier in *P-N* junction is ~ 0.5 *V* and the width of depletion region ~ 10^{-6} *m*.

So the barrier electric field $E = \frac{V}{d} = \frac{0.5}{10^{-6}} = 5 \times 10^5 \ V/m$

(3) **Some important graphs**

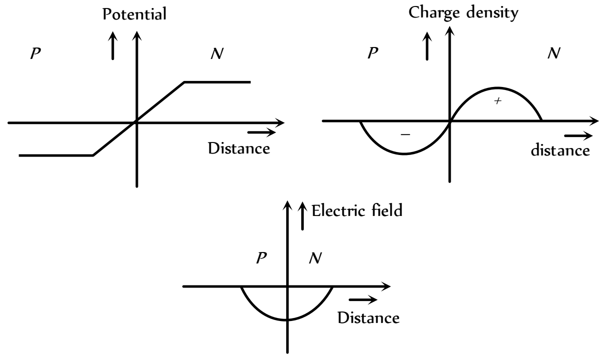


Fig. 27.19

(4) **Diffusion and drift current :** Because of concentration difference holes/electron try to diffuse from their side to other side. Only those holes/electrons crosses the junction, which have high kinetic energy. This diffusion results in an electric current from the *P*-side to the *N*-side known as diffusion current (i_{df})

As electron hole pair (because of thermal collisions) are continuously created in the depletion region. There is a regular flow of electrons towards the *N*-side and of holes towards the *P*-side. This makes a current from the *N*-side to the *P*-side. This current is called the drift current (i_{dr}).

Biasing

It means the way of connecting emf source to *P-N* junction diode. It is of following two types

(1) **Forward biasing :** Positive terminal of the battery is connected to the *P*-crystal and negative terminal of the battery is connected to *N*-crystal

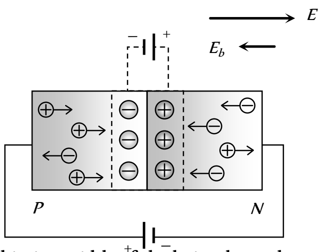


Fig. 27.20

(i) In forward biasing width of depletion layer decreases

(ii) In forward biasing resistance offered $R_{forward} \approx 10\Omega - 25\Omega$

(iii) Forward bias opposes the potential barrier and for $V > V_b$ a forward current is set up across the junction.

(iv) The current is given by $i = i_s(e^{eV/kT} - 1)$; where

i_s = Saturation current, In the exponent $e = 1.6 \times 10^{-}$ *C*,

k = Boltzmann's constant

(v) Cut-in (Knee) voltage : The voltage at which the current starts to increase rapidly. For *Ge* it is 0.3 *V* and for *Si* it is 0.7 *V*.

(vi) *df* – diffusion

dr – drift

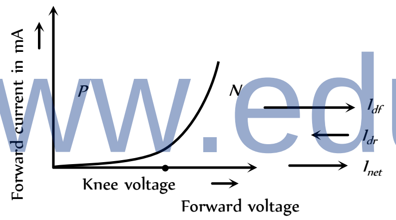


Fig. 27.21

(2) **Reverse biasing :** Positive terminal of the battery is connected to the *N*-crystal and negative terminal of the battery is connected to *P*-crystal

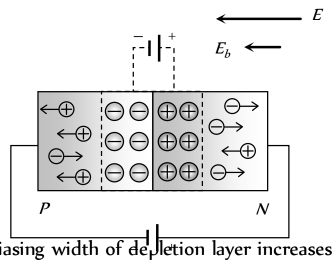


Fig. 27.22

(i) In reverse biasing width of depletion layer increases

(ii) In reverse biasing resistance offered $R_{reverse} \approx 10\Omega$

(iii) Reverse bias supports the potential barrier and no current flows across the junction due to the diffusion of the majority carriers.

(A very small reverse currents may exist in the circuit due to the drifting of minority carriers across the junction)

(iv) Break down voltage : Reverse voltage at which break down of semiconductor occurs. For *Ge* it is 25 *V* and for *Si* it is 35 *V*.

(v)

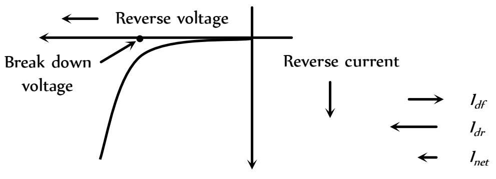


Fig. 27.23

Reverse Breakdown

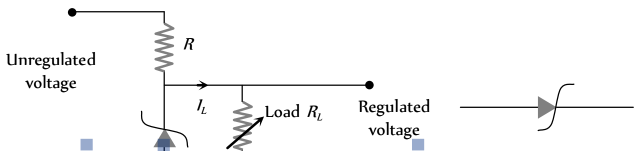
If the reverse biased voltage is too high, then breakdown of *P-N* junction diode occurs. It is of following two types

(1) **Zener breakdown :** When reverse bias is increased the electric field across the junction also increases. At some stage the electric field becomes so high that it breaks the covalent bonds creating electron, hole pairs. Thus a large number of carriers are generated. This causes a large current to flow. This mechanism is known as **Zener breakdown.**

(2) **Avalanche breakdown :** At high reverse voltage, due to high electric field, the minority charge carriers, while crossing the junction acquires very high velocities. These by collision breaks down the covalent bonds, generating more carriers. A chain reaction is established, giving rise to high current. This mechanism is called **avalanche breakdown.**

Special Purpose Diodes

(1) **Zener diode :** It is a highly doped *p-n* junction which is not damaged by high reverse current. It can operate continuously, without being damaged in the region of reverse background voltage. In the forward bias, the zener diode acts as ordinary diode. It can be used as voltage regulator



(A) Zener diode as a voltage regulator

(B) Symbol of zener diode

Fig. 27.24

(2) **Light emitting diode (LED :** Specially designed diodes, which give out light radiations when forward biases. LED'S are made of *GaAsp*, *Gap etc.*

These are forward biased *P-N*-junctions which emits spontaneous radiation.

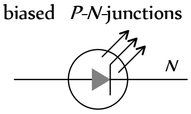


Fig. 27.25

(3) **Photo diode:** Photodiode is a special type of photo-detector. Suppose an optical photons of frequency ν is incident on a semiconductor, such that its energy is greater than the band gap of the semiconductor (*i.e.* $h\nu > E_g$) This photon will excite an electron from the valence band to the conduction band leaving a vacancy or hole in the valence band.

Which obviously increase the conductivity of the semiconductor. Therefore, by measuring the change in the conductance (or resistance) of the semiconductor, one can measure the intensity of the optical signal.

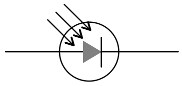


Fig. 27.26

(4) **Solar cells :** It is based on the photovoltic effect. One of the semiconductor region is made so thin that the light incident on it reaches the *P-N*-junction and gets absorbed. It converts solar energy into electrical energy.

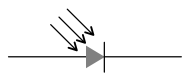


Fig. 27.27

P-N Junction Diode as a Rectifier

Rectifier is a circuit which converts *ac* to unidirectional pulsating output. In other words it converts *ac* to *dc*. It is of following two types

(1) **Half wave rectifier :** When the *P-N* junction diode rectifies half of the *ac* wave, it is called half wave rectifier

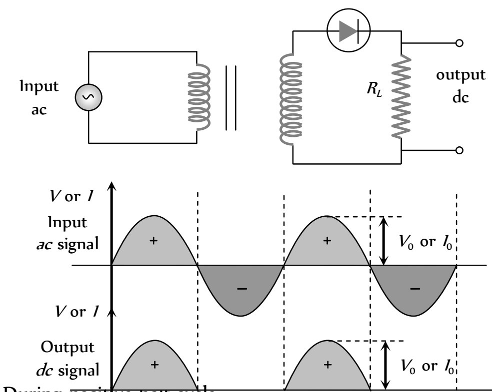


Fig. 27.28

(i) During positive half cycle

Diode ⟶ forward biased

Output signal ⟶ obtained

(ii) During negative half cycle

Diode ⟶ reverse biased

Output signal ⟶ not obtained

(iii) Output voltage is obtained across the load resistance R_L. It is not constant but pulsating (mixture of *ac* and *dc*) in nature .

(iv) Average output in one cycle

$$I_{dc}=\frac{I_0}{\pi} \text{ and } V_{dc}=\frac{V_0}{\pi};\ I_0=\frac{V_0}{r_f+R_L}$$

(r_f = forward biased resistance)

(v) r.m.s. output : $I_{rms}=\frac{I_0}{2}, V_{rms}=\frac{V_0}{2}$

(vi) The ratio of the effective alternating component of the output voltage or current to the *dc* component is known as ripple factor.

$$r=\frac{I_{ac}}{I_{dc}}=\left[\left(\frac{I_{rms}}{I_{dc}}\right)^2-1\right]^{1/2} = 1.21$$

(vii) Peak inverse voltage (PIV) : The maximum reverse biased voltage that can be applied before commoncement of Zener region is called the PIV. When diode is not conducting PIV across it = V_0

(viii) Efficiency : It is given by $\%\eta=\frac{P_{out}}{P_{in}}\times 100=\frac{40.6}{1+\frac{r_f}{R_L}}$

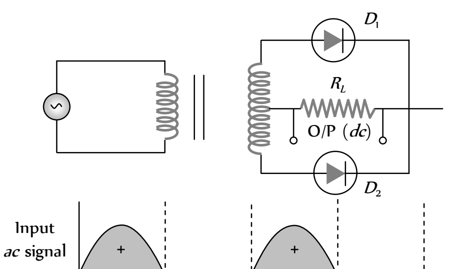
If $R_L >> r_f$ then η = 40.6%

If $R_L = r_f$ then η = 20.3%

(ix) Form factor = $\frac{I_{rms}}{I_{dc}}=\frac{\pi}{2}=1.57$

(x) The ripple frequency (ω) for half wave rectifier is same as that of *ac*.

(2) **Full wave rectifier :** It rectifies both halves of *ac* input signal.



(i) During positive half cycle

Diode : D forward biased

D ⟶ reverse biased

Output signal ⟶ obtained due to D only

(ii) During negative half cycle

Diode : D ⟶ reverse biased

D ⟶ forward biased

Output signal ⟶ obtained due to D only

(iii) Fluctuating *dc* ⟶ Filter ⟶ constant *dc*.

(iv) Output voltage is obtained across the load resistance R_L. It is not constant but pulsating in nature.

(v) Average output : $V_{av}=\frac{2V_0}{\pi}, I_{av}=\frac{2I_0}{\pi}$

(vi) *r.m.s.* output : $V_{rms}=\frac{V_0}{\sqrt{2}}, I_{rms}=\frac{I_0}{\sqrt{2}}$

(vii) Ripple factor : r = 0.48 = 48%

(viii) Ripple frequency : The ripple frequency of full wave rectifier = 2 × (Frequency of input *ac*)

(ix) Peak inverse voltage (PIV) : It's value is $2V_0$

(x) Efficiency : $\eta_{\%}=\frac{81.2}{1+\frac{r_f}{R_L}}$ for $r_f << R_L$, $\eta=81.2\%$

(3) **Full wave bridge rectifier :** Four diodes D, D, D and D are used in the circuit.

During positive half cycle D and D are forward biased and D and D are reverse biased

During negative half cycle D and D are forward biased and D and D are reverse biased

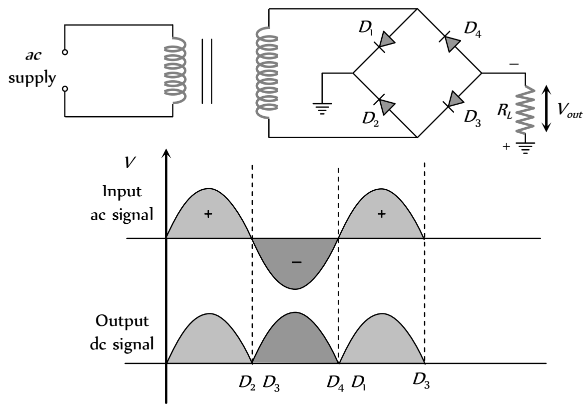


Fig. 27.30

Transistor

(1) The name of this electronic device is derived from it's fundamental action transfer resistor.

(2) Transistor does not need any heater or hot filament, transistor is small in size and light in weight.

(3) Transistor in general is known as bipolar junction transistor.

(4) Transistor is a current operated device.

(5) It consists of three main regions

(i) **Emitter** (*E*) **:** It provides majority charge carriers by which current flows in the transistor. Therefore the emitter semiconductor is heavily doped.

(ii) **Base** (*B*) **:** The based region is lightly doped and thin.

(iii) **Collector** (*C*) **:** The size of collector region is larger than the two other regions.

(6) Junction transistor are of two types :

(i) *NPN* transistor : It is formed by sandwiching a thin layer of *P*-type semiconductor between two *N*-type semiconductors

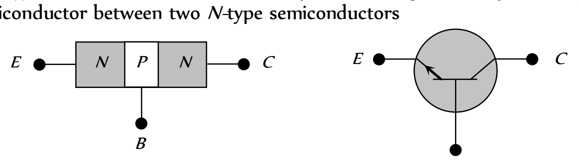


Fig. 27.31

In *NPN* transistor electrons are majority charge carriers and flow from emitter to base.

(ii) *PNP* transistor : It is formed by sandwiching a thin layer of *N*-type semiconductor between two *P*-type semiconductor

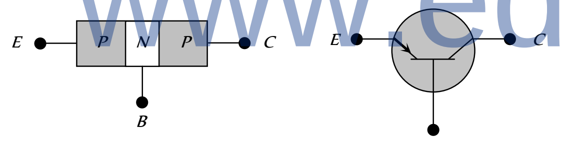


Fig. 27.32

In *PNP* transistor holes are majority charge carriers and flow from emitter to base.

In the symbols of both *NPN* and *PNP* transistor, arrow indicates the direction of conventional current.

Working of Transistor

(1) There are four possible ways of biasing the two *P-N* junctions (emitter junction and collector junction) of transistor.

(i) Active mode : Also known as linear mode operation.

(ii) Saturation mode : Maximum collector current flows and transistor acts as a closed switch from collector to emitter terminals.

(iii) Cut-off mode : Denotes operation like an open switch where only leakage current flows.

(iv) Inverse mode : The emitter and collector are inter changed.

Table 27.5 : Different modes of operation of a transistor

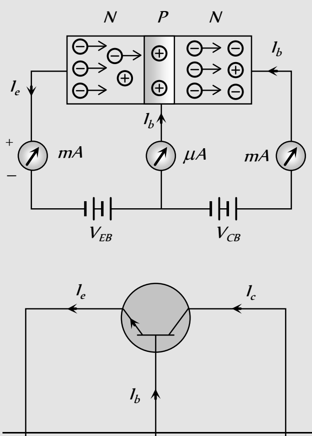
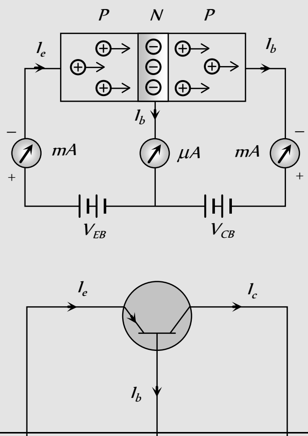
Operating mode	Emitter base bias	Collector base bias
Active	Forward	Reverse
Saturation	forward	Forward
Cut off	Reverse	Reverse
Inverse	Reverse	Forward

(2) A transistor is mostly used in the active region of operation *i.e.* emitter base junction is forward biased and collector base junction is reverse biased.

(3) From the operation of junction transistor it is found that when the current in emitter circuit changes. There is corresponding change in collector current.

(4) In each state of the transistor there is an input port and an output port. In general each electrical quantity (*V* or *I*) obtained at the output is controlled by the input.

Table 27.6 : Circuit diagram of *PNP*/*NPN* transistor

NPN – transistor	*PNP* – transistor
	
5% emitter electron combine with the holes in the base region resulting in small base current. Remaining 95% electrons enter the collector region.	5% emitter holes combine with the electrons in the base region resulting in small base current. Remaining 95% holes enter the collector region.
$I_e > I_c$, and $I_e = I_b + I_c$	$I_e > I_c$, and $I_e = I_b + I_c$

Transistor Configurations

A transistor can be connected in a circuit in the following three different configurations.

Common base (CB), Common emitter (CE) and Common collector (CC) configuration.

(i) **CB configurations :** Base is common to both emitter and collector .

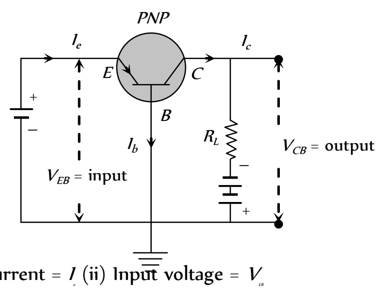


Fig. 27.33

(i) Input current = I_e (ii) Input voltage = V_{EB}

(iii) Output voltage = V_{CB} (iv) Output current = I_c

With small increase in emitter-base voltage V_{EB}, the emitter current I_e increases rapidly due to small input resistance.

(v) **Input characteristics :** If V_{CB} = constant, curve between I_e and V_{EB} is known as input characteristics. It is also known as emitter characteristics

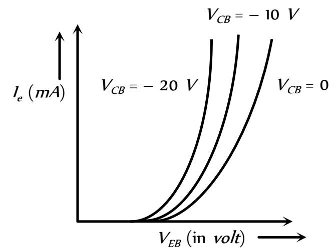


Fig. 27.34

Input characteristics of *NPN* transistor are also similar to the above figure but I_e and V_{eb} both are negative and V_{cb} is positive.

Dynamic input resistance of a transistor is given by

$$R_i = \left(\frac{\Delta V_{EB}}{\Delta I_e}\right)_{V_{CB}=\text{constant}} \qquad \{R_i \text{ is of the order of } 100\ \Omega\}$$

(vi) **Output characteristics :** Taking the emitter current i_e constant, the curve drawn between I_c and V_{cb} are known as output characteristics of *CB* configuration.

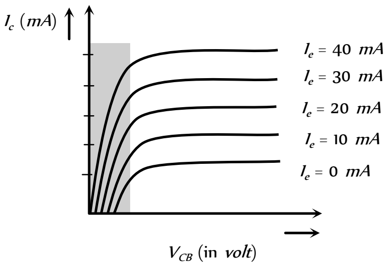


Fig. 27.35

Dynamic output resistance $R_o = \left(\frac{\Delta V_{CB}}{\Delta i_C}\right)_{i_e=\text{constant}}$

(2) **CE configurations :** Emitter is common to both base and collector.

The graphs between voltages and currents when emitter of a transistor is common to input and output circuits are known as CE characteristics of a transistor.

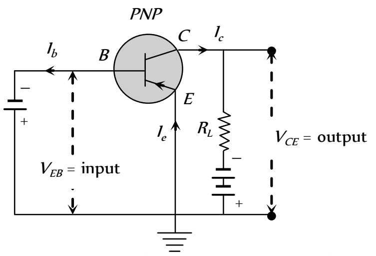


Fig. 27.36

Input characteristics : Input characteristic curve is drawn between base current I_b and emitter base voltage V_{eb} at constant collector emitter voltage V_{ce}.

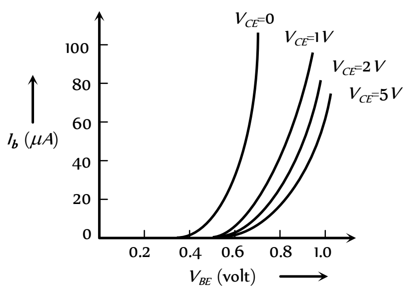


Fig. 27.37

Dynamic input resistance $R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}\rightarrow\text{constant}}$

Output characteristics : Variation of collector current I_c with V_{ce} can be noticed for V_{ce} between 0 to 1 *V* only. The value of V_{ce} up to which the I_c changes with V_{ce} is called knee voltage. The transistor are operated in the region above knee voltage.

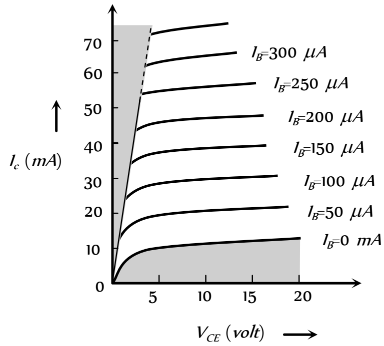


Fig. 27.38

Dynamic output resistance $R_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B\rightarrow\text{constant}}$

Field-Effect Transistor

The low input impedance of the junction transistor is a handicap in certain applications. In addition, it is difficult to incorporate large numbers of them in an integrated circuit and they consume relatively large amounts of power. The field-effect transistor (FET) lacks these disadvantages and is widely used today although slower in operation than junction transistors.

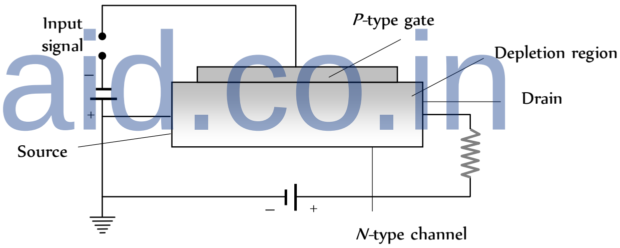


Fig. 27.39

An *n*-channel FET consists of a block of *N*-type material with contacts at each end together with a strip of *P*-type material on one side that is called the gate. When connected as shown, electrons move from the source terminal to the drain terminal through the *N*-type channel. the *PN* junction is given a reverse bias, and as a result both the *N* and *P* materials near the junction are depleted on charge carriers. The higher the reverse potential on the gate, the larger the depleted region in the channel and the fewer the electrons available to carry the current. Thus the gate voltage controls the channel current. Very little current passes through the gate circuit owing to the reverse bias, and the result is an extremely high input impedance. FET is uni-polar.

Transistor as an Amplifier

A device which increases the amplitude of the input signal is called amplifier.

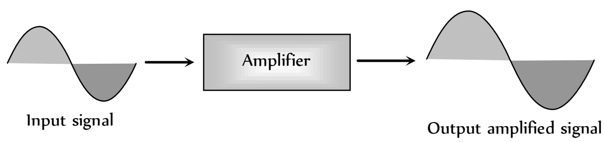


Fig. 27.40

The transistor can be used as an amplifier in the following three configuration

(i) CB amplifier (ii) CE amplifier (iii) CC amplifier

(1) ***NPN* transistor as CB amplifier**

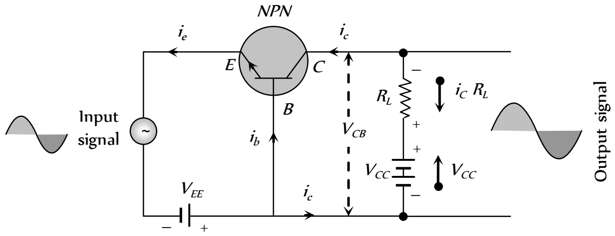


Fig. 27.41

(i) $i_e = i_b + i_C$; i_b = 5% of i_e and i_C = 95% of i_e

(ii) $V_{EE} < V_{CC}$

(iii) Net collector voltage $V_{CB} = V_{CC} - i_C R_L$

When the input signal (signal to be amplified) is fed to the emitter base circuit, it will change the emitter voltage and hence emitter current. This in turn will change the collector current (i_c). This will vary the collector voltage V_{CB}. This variation of V_{CB} will appear as an amplified output.

(iv) Input and output signals are in same phase

(2) ***NPN* transistor as *CE* amplifier**

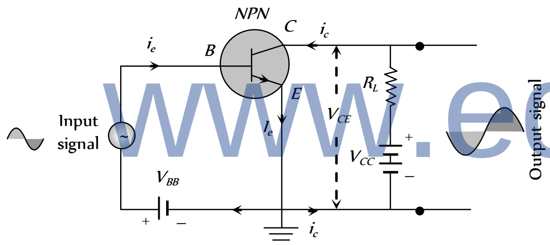


Fig. 27.42

(i) $i_e = i_b + i_C$; i_b = 5% of i_e and i_C = 95% of i_e

(ii) $V_{CC} > V_{BB}$

(iii) Net collector voltage $V_{CE} = V_{CC} - i_C R_L$

(iv) Input and output signals are 180° out of phase.

Different Gains in CE/CB Amplifiers

(1) **Transistor as CB amplifier**

(i) *ac* current gain $\alpha_{ac} = \dfrac{\text{Small change in collector current } (\Delta i_c)}{\text{Small change in collector current } (\Delta i_e)}$

V_{CB} (constant)

(ii) *dc* current gain $\alpha_{dc} (\text{or } \alpha) = \dfrac{\text{Collector current} (i_c)}{\text{Emitter current } (i_e)}$

valve of α lies between 0.95 to 0.99

(iii) Voltage gain $A_v = \dfrac{\text{Change in output voltage} (\Delta V_o)}{\text{Change in input voltage} (\Delta V_i)}$

$\Rightarrow A_v = \alpha_{ac} \times$ Resistance gain

(iv) $\text{Power gain} = \dfrac{\text{Change in output power} (\Delta P_o)}{\text{Change in input power} (\Delta P_c)}$

$\Rightarrow \text{Power gain} = \alpha_{ac}^2 \times \text{Resistance gain}$

(2) **Transistor as CE amplifier**

(i) *ac* current gain $\beta_{ac} = \left(\dfrac{\Delta i_c}{\Delta i_b}\right)$ V_{CE} = constant

(ii) *dc* current gain $\beta_{dc} = \dfrac{i_c}{i_b}$

(iii) Voltage gain : $A_v = \dfrac{\Delta V_o}{\Delta V_i} = \beta_{ac} \times \text{Resistance gain}$

(iv) $\text{Power gain} = \dfrac{\Delta P_o}{\Delta P_i} = \beta_{ac}^2 \times \text{Resistance gain}$

(v) Trans conductance (g_m) : The ratio of the change in collector current to the change in emitter base voltage is called trans conductance. *i.e.* $g_m = \dfrac{\Delta i_c}{\Delta V_{EB}}$. Also $g_m = \dfrac{A_V}{R_L}$; R_L = Load resistance

(3) **Relation between α and β** : $\beta = \dfrac{\alpha}{1-\alpha}$ or $\alpha = \dfrac{\beta}{1+\beta}$

Transistor as an Oscillator

(1) It is defined as a circuit which generates an *ac* output signal without any externally applied input signal.

Audio frequency oscillators generates signals of frequencies ranging from a few *Hz* to 20 *kHz* and radio frequency oscillators have a range from few *kHz* to *MHz*.

(2) In an oscillator the frequency, waveform, and magnitude of *ac* power generated is controlled by circuit itself.

(3) An oscillator may be considered as amplifier which provides it's own input signal.

(4) The essential of a transistor oscillator are

(i) **Tank circuit :** Parallel combination of *L* and *C*. This network resonates at a frequency $\nu_0 = \dfrac{1}{2\pi}\sqrt{\dfrac{1}{LC}}$.

(ii) **Amplifier :** It receives *dc* power from the battery and converts into *ac* power.

The amplifier increases the strength of oscillations.

(iii) **Feed back circuit :** This circuit supplies a part of the collector energy to the tank circuit.

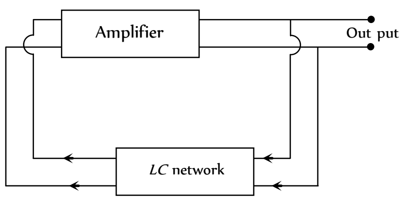


Fig. 27.43

(5) A basic common-emitter *NPN* oscillator is shown in the figure.

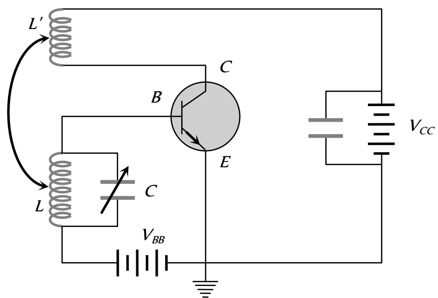


Fig. 27.44

A tank circuit (*L-C* circuit) is connected in the base-emitter circuit, in which the capacitance *C* is kept variable. By changing *C* oscillations of a desired frequency can be obtained. An inductance coil *L'* connected in the collector-emitter circuit is coupled to coil *L*.

On completion of the circuit electrical oscillations are developed in the tank circuit. The circuit amplifies these oscillations. A part of the amplifies signal in the collector circuit is fed back in the base circuit by the coupling between *L* and *L'*. Due to this feed back amplitude of oscillation builds up till power dissipation in the oscillatory circuit becomes equal to power fed-back. In this state the amplitude of oscillations becomes constant.

The oscillations can be transferred to an external circuit by mutual induction in a coil connected in that circuit.

(6) **Need for positive feedback :** The oscillations are damped due to the presence of some inherent electrical resistance in the circuit. Consequently, the amplitude of oscillations decreases rapidly and the oscillations ultimately stop. Such oscillations are of little practical importance. In order to obtain oscillations of constant amplitude, we make an arrangement for regenerative or positive feedback from the output circuit to the input circuit so that the losses in the circuit can be compensated.

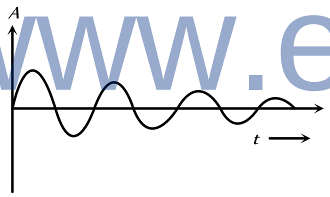


Fig. 27.45

Table 27.7: Comparison between CB, CE and CC amplifier

Characteristic	Amplifier		
	CB	CE	CC
Input resistance (R_i)	≈ 50 to 200 Ω low	≈ 1 to 2 kΩ medium	≈ 150 – 800 kΩ high
Output resistance (R_o)	≈ 1 – 2 kΩ high	≈ 50 kΩ medium	≈ kΩ low
Current gain	0.8 – 0.9 low	20 – 200 high	20 – 200 high
Voltage gain	Medium	High	Low
Power gain	Medium	High	Low
Phase difference between input and output voltages	Zero	180°	Zero
Used as amplifier for	current	Power	Voltage

Digital Electronics

Decimal and Binary Number System

(1) **Decimal number system :** In a decimal number system, we have ten digits *i.e.* 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

A decimal number system has a base of ten (10)

e.g. 1971 = 1000 + 900 + 70 + 1

= $1 \times 10^3 + 9 \times 10^2 + 7 \times 10^1 + 1 \times 10^0$

MSD LSD

LSD = Least significant digit

MSD = Most significant digit

(2) **Binary number system :** A number system which has only two digits *i.e.* 0 (Low) and 1 (High) is known as binary system. The base of binary number system is 2.

(i) Each digit in binary system is known as a bit and a group of bits is known as a byte.

(ii) The electrical circuit which operates only in these two state *i.e.* 1 (On or High) and 0 (*i.e.* Off or Low) are known as digital circuits.

Table 27. 8 : Different names for the digital signals

State Code	1	0
Name for the State	On	Off
	Up	Down
	Close	Open
	Excited	Unexcited
	True	False
	Pulse	No pulse
	High	Low
	Yes	No

(3) **Decimal to binary conversion**

(i) Divide the given decimal number by 2 and the successive quotients by 2 till the quotient becomes zero.

(ii) The sequence of remainders obtained during divisions gives the binary equivalent of decimal number.

(iii) the most significant digit (or bit) of the binary number so obtained is the last remainder and the least significant digit (or bit) is the first remainder obtained during the division.

***For Example* :** Binary equivalence of 61

2	61	Remainder
2	30	1 LSD
2	15	0

2	7	1
2	3	1
2	1	1
	0	1 MSD

$\Rightarrow (61)_{10} = (111101)_2$

(4) **Binary to decimal conversion :** The least significant digit in the binary number is the coefficient of 2 with power zero. As we move towards the left side of LSD, the power of 2 goes on increasing.

For Example **:** $(11111100101)_2 = 1 \times 2^{10} + 1 \times 2^9 + 1 \times 2^8 + 1 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 2021$

Voltage Signal

(1) **Analogue voltage signal :** The signal which represents the continuous variation of voltage with time is known as analogue voltage signal

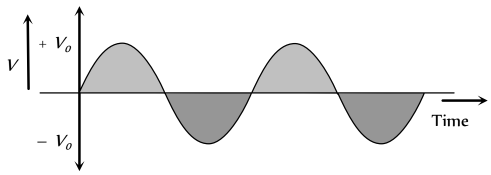


Fig. 27.46

(2) **Digital voltage signal :** The signal which has only two values. *i.e.* either a constant high value of voltage or zero value is called digital voltage signal

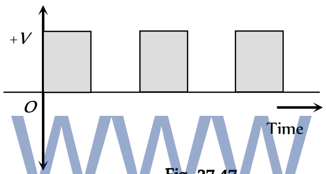


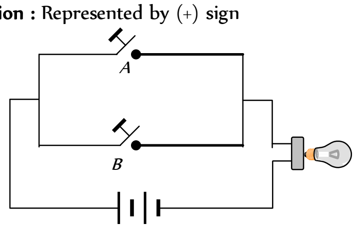
Fig. 27.47

Boolean Algebra

(1) In Boolean algebra only two states of variables (0 and 1) are allowed.

(2) The variables (A, B, C ....) of Boolean Algebra are subjected to three operations.

(i) **OR Operation :** Represented by (+) sign



Boolean expression $Y = A + B$

Fig. 27.48

When switch A or B is closed – Bulb glows

(ii) **AND Operation :** Represented by (·) sign

Boolean expression $Y = A \cdot B$

When switches A and B both are closed – Bulb glows

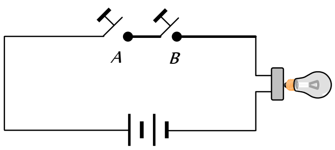
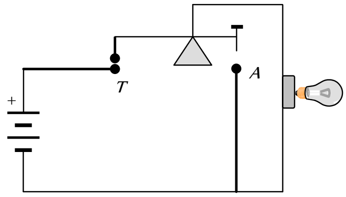


Fig. 27.49

(iii) **NOT Operation :** Represented by bar over the variables

Boolean expression $Y = \overline{A}$



A OFF → Lamp ON

A ON → Contact at T is broken → Lamp OFF

Fig. 27.50

(3) **Basic Boolean postulates and laws**

(i) Boolean Postulates : $0 + A = A$, $1 \cdot A = A$,

$1 + A = 1$, $0 \cdot A = 0$,

$A + \overline{A} = 1$

(ii) Identity law : $A + A = A$, $A \cdot A = A$

(iii) Negation law : $\overline{\overline{A}} = A$

(iv) Commutative law : $A + B = B + A$, $A \cdot B = B \cdot A$

(v) Associative law : $(A+B) + C = A + (B+C)$,

$(A \cdot B) \cdot C = A \cdot (B \cdot C)$

(vi) Distributive law : $A \cdot (B+C) = A \cdot B + A \cdot C$

$(A + B) \cdot (A + C) = A + BC$

(vii) Absorption laws : $A + A \cdot B = A$, $A \cdot (A + B) = A$

$\overline{A} \cdot (A + B) = \overline{A} \cdot B$

(viii) Boolean identities : $A + \overline{A}B = A + B$, $A(\overline{A} + B) = AB$,

$A + BC = (A + B)(A + C)$, $(\overline{A} + B) \cdot (A + C) = \overline{A}C + AB$

(ix) **De Morgan's theorem :** It states that the complement of the whole sum is equal to the product of individual complements and vice versa *i.e.* $\overline{A + B} = \overline{A} \cdot \overline{B}$ and $\overline{A \cdot B} = \overline{A} + \overline{B}$

Logic Gates and Truth Table

(1) **Logic gate :** The digital circuit that can be analysed with the help of Boolean algebra is called logic gate or logic circuit. A logic gate has two or more inputs but only one output.

There are primarily three logic gates namely the OR gate, the AND gate and the NOT gate.

(2) **Truth table :** The operation of a logic gate or circuit can be represented in a table which contains all possible inputs and their corresponding outputs is called the truth table. To write the truth table we use binary digits 1 and 0.

The 'OR' Gate

(1) It has two inputs (A and B) and only one output (Y)

(2) Boolean expression is $Y = A + B$ and is read as "Y equals A **OR** B"

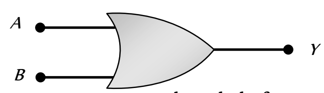
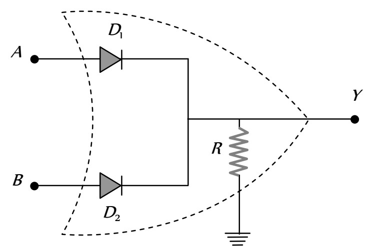


Fig. 27.51 : Logical symbol of OR gate

(3) **Realization of OR gate**



(i) $A = 0$, $B = 0$

Both diodes D_1 and D_2 do not conduct and hence $Y = 0$

(ii) $A = 0$, $B = 1$

D_1 = Does not conducts, D_2 = Conducts, hence $Y = 1$

(iii) $A = 1$, $B = 0$

D_1 = Conducts, D_2 = Does not conduct, hence $Y = 1$

(iv) $A = 1$, $B = 1$

Both D_1 and D_2 conducts, hence $Y = 1$

(4) **Truth table for 'OR' gate**

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

The 'AND' Gate

(1) It has two inputs (A and B) and only one output (Y)

(2) Boolean expression is $Y = A \cdot B$ is read as " Y equals A AND B"

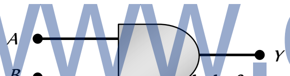


Fig. 27.53 : Logical symbol of AND gate

(3) **Realization of AND gate**

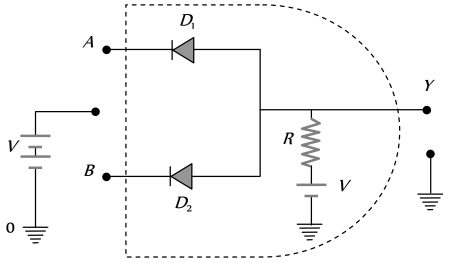


Fig. 27.54

(i) $A = 0$, $B = 0$

The voltage supply through R is forward biasing diodes D_1 and D_2 (offers low resistance) the voltage V would drop across R

The output voltage at Y = the voltage across diode = 0

(ii) $A = 0$, $B = 1$

D_1 = conducts, D_2 = Not Conducts

the out voltage at Y= The voltage across the diode (D) =0

(iii) $A = 1$, $B = 0$

D_1 = Conducts, D_2 = Not conducts

the out voltage at Y= The voltage across the diode (D_1) =0

iv) $A = 1$, $B = 1$

None of the diode conducts

the out voltage at Y= Battery voltage =1

(4) **Truth table for 'AND' gate**

A	B	$Y = A . B$
0	0	0
0	1	0
1	0	0
1	1	1

The 'NOT' Gate

(1) It has only one input and only one output.

(2) Boolean expression is $Y = \overline{A}$ and is read as "y equals not A"

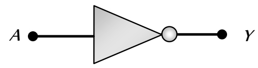


Fig 27.55 : Logical symbol of NOT gate

(3) **Realization of NOT gate :** The transistor is so biased that the collector voltage $V_{cc} = V$ (Voltage corresponding to 1 state)

The resistors R and R_1 are so chosen that if the input is low *i.e.* O, the transistor is in the cut off and hence the voltage appearing at the output will be the same as applied V. Hence $Y = V$ (or state 1)

If the input is high, the transistor current is in saturation and the net voltage at the output Y is 0 (in state 0)

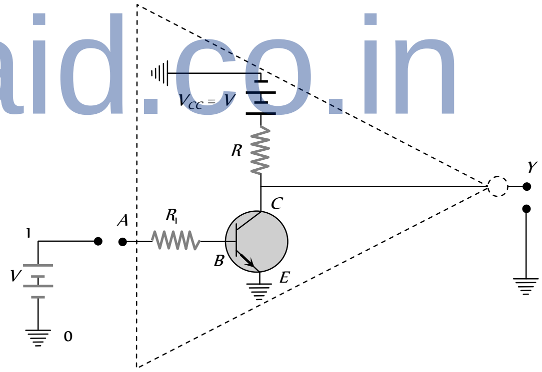


Fig. 27.56

(4) **Truth table for NOT gate**

A	$Y = \overline{A}$
0	1
1	0

Combination of Logic Gates

(1) **The 'NAND' gate :** From 'AND' and 'NOT' gate

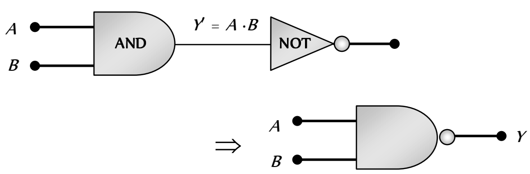


Fig. 27.57

Boolean expression and truth table : $Y = \overline{A \cdot B}$

A	B	$Y = A \cdot B$	Y
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

(2) **The 'NOR' gate :** From 'OR' and 'NOT' gate

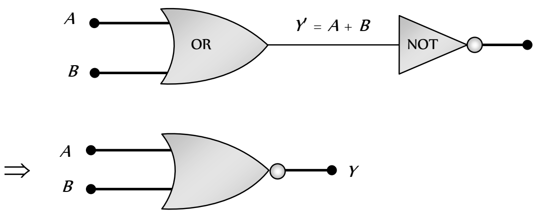


Fig. 27.58

Boolean expression and truth table : $Y = \overline{A + B}$

A	B	$Y = A + B$	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(3) **The 'XOR' gate :** From 'NOT', 'AND' and 'OR' gate. Known as exclusive OR gate.

or

The logic gate which gives high output (*i.e.,* 1) if either input A or input B but not both are high (*i.e.* 1) is called exclusive OR gate or the XOR gate.

It may be noted that if both the inputs of the XOR gate are high, then the output is low (*i.e.,* 0).

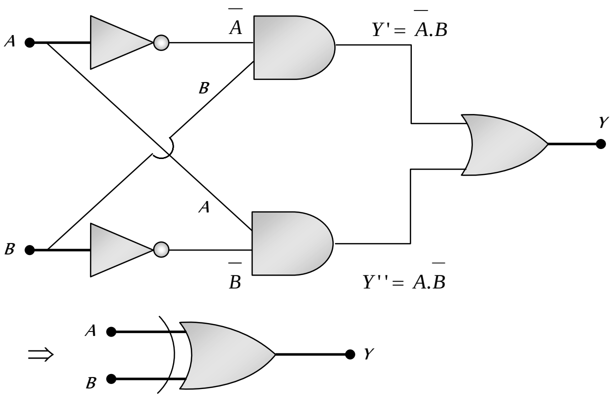


Fig. 27.59

Boolean expression and truth table : $Y = A \oplus B = \bar{A}B + A\bar{B}$

A	B	Y
0	0	0
0	1	1

1	0	1
1	1	0

(4) **The exclusive nor (XNOR) gate**

XOR + NOT ⟶ XNOR

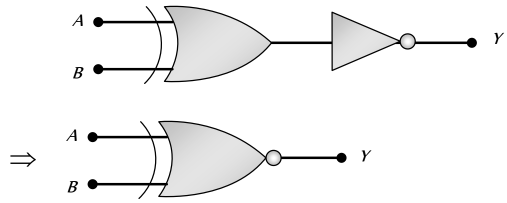


Fig. 27.60

Boolean expression : $Y = A \odot B = \bar{A}\,\bar{B} + AB$

Logic Gates Using 'NAND' Gate

The NAND gate is the building block of the digital electronics. All the logic gates like the OR, the AND and the NOT can be constructed from the NAND gates.

(1) **Construction of the 'NOT' gate from the 'NAND' gate**

(i) When both the inputs (A and B) of the NAND gate are joined together then it works as the NOT gate.

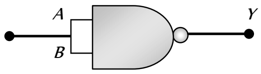


Fig. 27.61

(ii) Truth table and logic symbol

Input	Output
$A = B$	Y
0	1
1	0

(2) **Construction of the 'AND' gate from the 'NAND' gate**

(i) When the output of the NAND gate is given to the input of the NOT gate (made from the NAND gate), then the resultant logic gate works as the AND gate

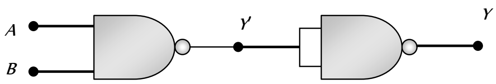


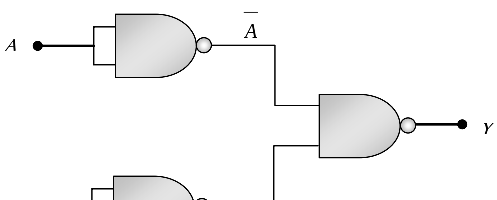
Fig. 27.62

(ii) Truth table and logic symbol

A	B	Y	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

(3) **Construction of the 'OR' gate by the 'NAND' gate**

(i) When the outputs of two NOT gates (obtained from the NAND gate) is given to the inputs of the NAND gate, the resultant logic gate works as the OR gate



(ii) Truth table and logic symbol

A	B	$\overline{A}$	$\overline{B}$	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

Valve Electronics

Electron Emission from Metal

(1) Free electron in metal experiences a barrier on surface due to attractive Coulombian force.

(2) When kinetic energy of electron becomes greater than barrier potential energy (or binding energy E_b) then electron can come out of the surface of metal.

(3) **Fermi energy (E_f) :** Is the maximum possible energy possessed by free electron in metal at 0K temperature

(i) In this energy level, probability of finding electron is 50%.

(ii) This is a reference level and it is different for different metals.

(4) **Threshold energy (or work function W_0) :** Is the minimum energy required to take out an electron from the surface of metal. Also $W_0 = E_b - E_f$

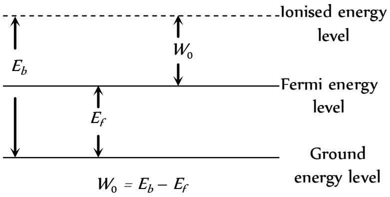


Fig. 27.64

Work function for different materials

$(W_0)_{\text{Pure tungsten}} = 4.5\ eV$

$(W_0)_{\text{Thoriated tungsten}} = 2.6\ eV$

$(W_0)_{\text{Oxide coated tungsten}} = 1\ eV$

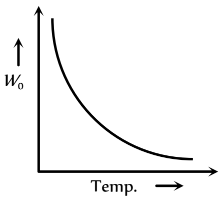


Fig. 27.65

(5) Four processes of electron emission from a metal are

(i) Thermionic emission

(ii) Photoelectric emission

(iii) Field emission

(iv) Secondary emission

Thermionic Emission

(1) The phenomenon of ejection of electrons from a metal surface by the application of heat is called thermionic emission and emitted electrons are called thermions and current flowing is called thermion current.

(2) Thermions have different velocities.

(3) This was discovered by Edison

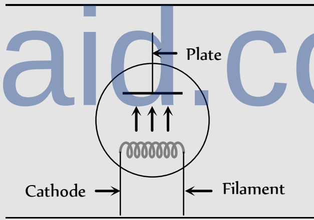
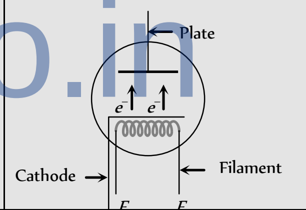
(4) Richardson – Dushman equation for current density (*i.e.* electric current emitted per unit area of metal surface) is given as $J = AT^2 e^{-W_0/kT} = AT^2 e^{-\frac{qV}{kT}} = AT^2 e^{-\frac{11600\ V}{T}}$

where A = emission constant = $12 \times 10^4\ amp/m^2\text{-}K^2$, k = Boltzmann's constant, T = Absolute temp and W_0 = work function.

(5) The number of thermions emitted per second per unit area (J) depends upon following :

(i) $J \propto T^2$ (ii) $J \propto e^{-W_0}$

Table 27.9: Types of thermionic emitters

Directly heated emitter	Indirectly heated emitter
	
Cathode is directly heated by passing current.	Cathode is indirectly heated.
Thermionic current is less.	Thermionic current is more.
Energy consumption and life is small.	Energy consumption and life is more.

Vacuum Tubes and Thermionic Valves

(1) Those tubes in which electrons flows in vacuum are called vacuum tubes.

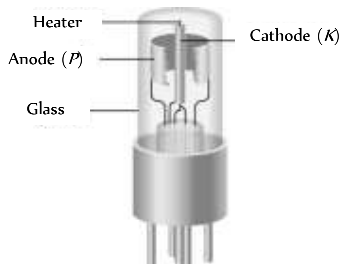
(2) These are also called valves because current flow in them is unidirectional.

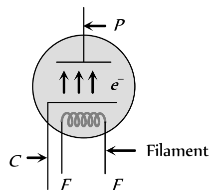
(3) Vacuum in vacuum tubes prevents the emission of secondary electrons and burning of heated filament (which will happen if we use air in place of vacuum)

(4) Every vacuum tube necessarily contains two electrodes out of which one is always electron emitter (cathode) and another one is electron collector (anode or plate).

(5) Depending upon the number of electrodes used the vacuum tubes are named as diode, triode, tetrode, pentode.... respectively, if the number of electrodes used are 2, 3, 4, 5..... respectively.

Diode Valve





(1) **Inventor :** Fleming

(2) **Principle :** Thermionic emission

(3) **Number of electrodes :** Two

(4) **Working :** When plate potential (V_p) is positive, plate current (i_p) flows in the circuit (because some emitted electrons reaches to plate). If $+V_p$ increases i_p also increases and finally becomes maximum (saturation).

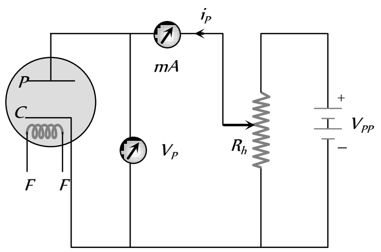


Fig. 27.67

(5) **Space charge :** If V_p is zero or negative, then electrons collect around the plate as a cloud which is called space charge. space charge decreases the emission of electrons from the cathode.

Characteristic Curves of a Diode

A graph represents the variation of i_p with V_p at a given filament current (i_f) is known as characteristic curve.

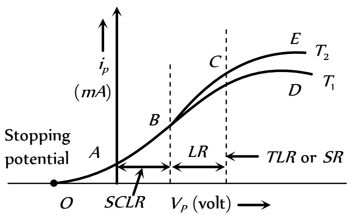


Fig. 27.68

The curve is not linear hence diode valve is a non-ohmic device.

(1) **Space charge limited region (SCLR) :** In this region current is space charge limited current.

Also $i_p \propto V_p^{3/2} \Rightarrow i_p = kV_p^{3/2}$; where k is a constant depending on metal as well as on the shape and area of the cathode. This is called child's law.

(2) **Linear region (LR) :** In this region $i_p \propto V_p$

(3) **Saturated region (SR) or temperature limited region (TLR) :** In this part, the current is independent of potential difference applied between the cathode and anode.

$i_p \neq f(V_p)$, $i_p = f$ (Temperature)

The saturation current follows Richardson Dushman equation *i.e.* $i = AST^2 e^{-\phi_0/kT}$; Here

A = Emission constant = $\dfrac{4\pi mek^2}{h^3} amp/m^2 - k^2$

S = Area of emitter in m^2 ; T = Absolute temperature in K

ϕ_0 =Work function of metal in Joule; k =Boltzmann constant

The small increase in i_p after saturation stage due to field emission is known as Shottkey effect.

(4) **Diode resistance**

(i) Static plate resistance or dc plate resistance : $R_p = \dfrac{V_p}{i_p}$.

(ii) Dynamic or ac plate resistance : If at constant filament current, a small change ΔV_p in the plate potential produces a small change Δi_p in the plate current, then the ratio $\Delta V_p / \Delta i_p$ is called the dynamic resistance, or the 'plate resistance' of the diode $r_p = \dfrac{\Delta V_p}{\Delta i_p}$.

(iii) In SCLR : $r_p < R_p$, (iv) In TLR : $R_p < r_p$ and $r_p = \infty$.

(5) **Uses of diode valve**

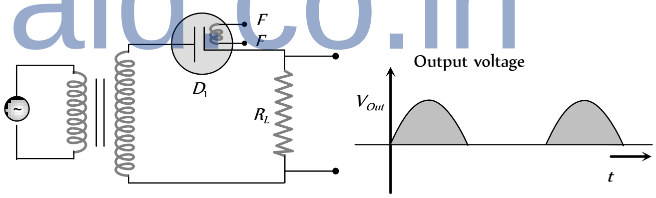
(i) As a rectifier (ii) As a detector

(iii) As a transmitter (iv) As a modulator

Diode Valve as a Rectifier

Rectifier is a device which converts ac into dc

(1) **Half wave rectifier :** The circuit of half wave rectifier is shown below. In the first half cycle of *ac* input the diode conducts and in the second half cycle it does not conducts. Thus half of the input cycle appear as output.



(A) Half wave rectifier (B) Output signal

Fig. 27.69

(i) Output voltage is not constant but pulsating in nature.

(ii) It is a mixture of *ac* and *dc.*

(iii) The *dc* values of the half wave output are given by

$$V_{d.c.} = \frac{V_0}{\pi} \text{ and } i_{d.c.} = \frac{i_0}{\pi}$$

(iv) The *r.m.s.* values of the half wave output are given by

$$V_{rms} = \frac{V_0}{2} \text{ and } i_{rms} = \frac{i_0}{2}$$

(v) The ratio of the effective alternating component to the direct component of the output voltage or current is called ripple factor

$$r = \frac{i_{a.c.}}{i_{d.c.}} = \sqrt{\left(\frac{i_{rms}}{i_{d.c.}}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2}\right)^2 - 1} = 1.21 = 121\%.$$

(vi) Efficiency of half wave rectifier is given by

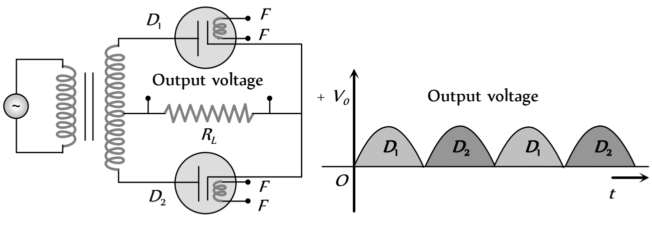
$$\eta = \frac{P_{d.c.}}{P_{a.c.}} \times 100\% = \frac{40.6}{1+\frac{r_p}{R_L}}\%$$

The maximum efficiency (for $R_L >> r_p$) = 40.6%

(vii) Form factor $= \frac{i_{rms}}{i_{d.c.}} = \frac{V_{rms}}{V_{d.c.}} = \frac{\pi}{2} = 1.57$

(viii) Ripple frequency = Frequency of input ac = ω

(2) **Full wave rectifier :** It consist of two diodes D_1 and D_2. They conducts alternately during positive and negative half cycle of input *ac* and a unidirectional (or *dc*) current flows in output



(A) Full wave rectifier (B) Output signal

Fig. 27.70

(i) The average or *dc* output values are

$$V_{d.c.} = \frac{2V_0}{\pi} \text{ and } i_{d.c.} = \frac{2i_0}{\pi}$$

(ii) It is a mixture of *ac* and *dc*

(iii) The *r.m.s.* values of the half wave output are given by

$$V_{rms} = \frac{V_0}{\sqrt{2}} \text{ and } i_{rms} = \frac{i_0}{\sqrt{2}}$$

(iv) Ripple factor $r = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1} = 0.48 = 48\%$.

(v) Efficiency of half wave rectifier is given by

$$\eta = \frac{P_{d.c.}}{P_{a.c.}} \times 100\% = \frac{81.2}{1+\frac{r_p}{R_L}}\%$$

The maximum efficiency (for $R_L >> r_p$) = 81.2%

(vii) Form factor $= \frac{i_{rms}}{i_{d.c.}} = \frac{V_{rms}}{V_{d.c.}} = \frac{\pi}{2\sqrt{2}} = 1.11$

(viii) Ripple frequency = Double of frequency of input ac = 2ω

Filter Circuit

Filter circuits smooth out the fluctuations in amplitude of ac ripple of the output voltage obtained from a rectifier.

(i) Filter circuit consists of capacitors or/ and choke coils.

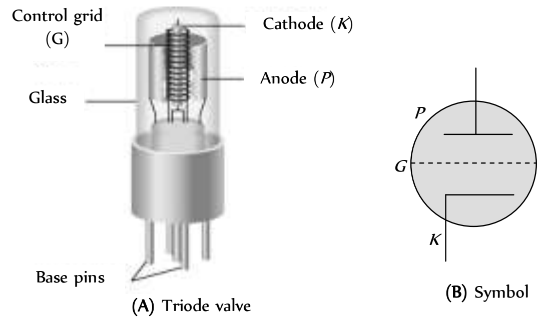
(ii) A capacitor offers a high resistance to low frequency ac ripple (infinite resistance to dc) and a low resistance to high frequency ac ripple. Therefore, it is always used as a shunt to the load.

(iii) A choke coil offers high resistance to high frequency ac, and almost zero resistance to dc. It is used in series.

(iv) π - Filter is best for ripple control.

(v) For voltage regulation choke input filter (*L*-filter) is best.

Triode Valve



(A) Triode valve (B) Symbol

Fig. 27.71

(1) **Inventor :** Dr. Lee De Forest

(2) **Principle :** Thermionic emission

(3) **Number of electrodes :** It consists of three electrodes.

(i) Filament (*F*) : It emits electron on heating.

(ii) Plate or anode (*P*) : It collect the electrons.

(iii) Control grid : It is a third electrode, also known as control grid, which controls the electrons going from cathode to plate. As a result grid controls the plate current. It is kept near the cathode with low negative potential.

When grid is given positive potential then plate current increases but in this case triode cannot be used for amplifier and therefore grid is normally not given positive potential.

When grid is given negative potential then plate current decreases but in this case grid controls plate current most effectively.

(4) **Working :** Plate of triode valve is always kept at positive potential *w.r.t.* cathode. The potential of plate is more than that of grid.

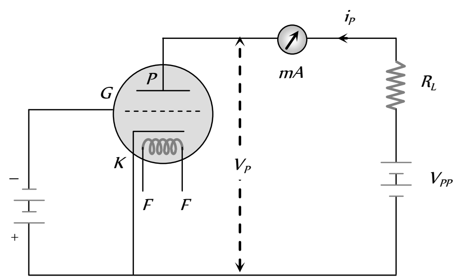


Fig. 27.72

The variation of plate potential affects the plate current as follows $i_p = k\left(V_G + \frac{V_p}{\mu}\right)^{3/2}$; where μ = Amplification factor of triode valve, k = Constant of triode valve.

The valve of V_G for which the plate current becomes zero is known as the cut off voltage. For a given V_p, it is given by $V_G = -\frac{V_p}{\mu}$.

Characteristics of Triode

The triode characteristics can be obtained under two sets of condition as

Static characteristics and dynamic characteristics

(1) **Static characteristics :** Graphical representation of V_p or V_g and i_p without any load

(i) **Static plate characteristic curve :** Graphical representation of i_p and V_p at constant V_g.

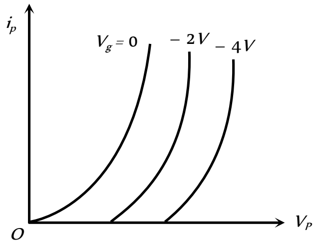


Fig. 27.73

(ii) **Static mutual characteristics curve :** Graphical representation of i_p and V_g when V_p is kept constant

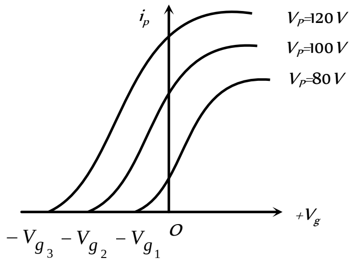


Fig. 27.74

(iii) **Constant current characteristic curve :** Graphical representation between V_p and V_g when i_p is constant.

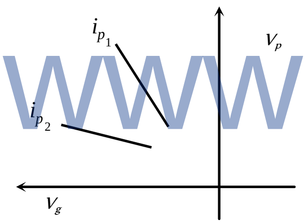


Fig. 27.75

(2) **Dynamic characteristics :** The curve plotted between i_p, V_g and V_p when the triode contains load in the plate circuit are called dynamics characteristics of diode.

(i) **Load line :** Voltage drop i_pR_L across load R_L which decreases the plate potential will be less then the supply voltage.

Plate voltage $V_p = V_{pp} - i_pR_L \Rightarrow i_p = -\frac{1}{R_L}V_p + \frac{V_{pp}}{R_L}$

This equation represents a straight line on the static plate characteristics, joining the points $(V_{pp}, 0)$ on plate voltage axis and $(0, V_{pp}/R_L)$ on plate current axis. This line known as load line.

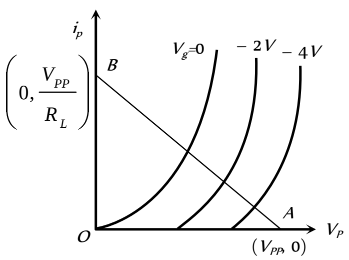


Fig. 27.76

(a) Points at which load line cuts the plate characteristic curves are called operating points.

(b) The slope of load line $AB = \frac{di_p}{dV_p} = -\frac{1}{R_L}$

(c) In graph, $OA = V_{pp}$ = intercept of load line on V_p axis and $OB = V_{pp}/R_L$ = intercept of load line on i_p axis.

(d) Static plate characteristic + load line

⟶ Dynamic plate characteristic

Static mutual characteristic + load line

⟶ Dynamic mutual characteristic

Constants of Triode Valve

(1) **Plate or dynamic resistance (r_p)**

(i) The slope of plate characteristic curve is equal to $\frac{1}{\text{plate resistance}}$

or It is the ratio of small change in plate voltage to the change in plate current produced by it, the grid voltage remaining constant. That is, $r_p = \frac{\Delta V_p}{\Delta i_p}, V_G = \text{constant}$.

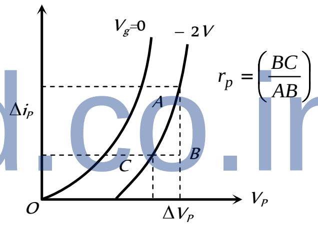


Fig. 27.77

(ii) It is expressed in kilo ohms ($K\Omega$). Typically, it ranges from $8K\Omega$ to $40K\Omega$. The r_p can be determined from plate characteristics. It represents the reciprocal of the slope of the plate characteristic curve.

(iii) If the distance between plate and cathode is increased the r_p increases. The value of r_p is infinity in the state of cut off bias or saturation state.

(2) **Mutual conductance (or *trans* conductance) (g_m)**

(i) It is defined as the ratio of small change in plate current (Δi_p) to the corresponding small change in grid potential (ΔV_g) when plate potential V_p is kept constant *i.e.* $g_m = \left(\frac{\Delta i_p}{\Delta V_g}\right)_{V_p \text{ is constant}}$

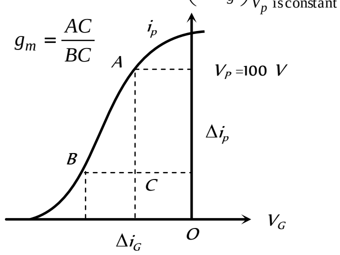


Fig. 27.78

(ii) The value of g_m is equal to the slope of mutual characteristics of triode.

(iii) The value of g_m depends upon the separation between grid and cathode. The smaller is this separation, the larger is the value of g_m and vice versa.

(iv) In the saturation state, the value of $\Delta i_p = 0$, $g_m = 0$

(3) **Amplification factor (μ) :** It is defined as the ratio of change in plate potential (ΔV_p) to produce certain change in plate current (Δi_p) to the change in grid potential (ΔV_g) for the same change in plate current (Δi_p) *i.e.* $\mu = -\left(\frac{\Delta V_p}{\Delta V_g}\right)_{\Delta I_p = \text{a constant}}$; negative sign indicates that V_p and V_g are in opposite phase.

(i) Amplification factor depends upon the distance between plate and cathode (d_{pk}), plate and grid (d_{pg}) and grid and cathode(d_{gk}).

$$i.e.\ \mu \propto d_{pg} \propto d_{pk} \propto \frac{1}{d_{gk}}$$

(ii) The value of μ is greater than one.

(iii) Amplification factor is unitless and dimensionless.

(4) **Relation between triode constants :** The triode constants are not independent of each other. They are related by the relation $\mu = r_p \times g_m$

The r_p and g_m depends on i_p in the following manner

$$r_p \propto i_p^{-1/3},\ g_m \propto i_p^{1/3},\ \mu \text{ does not depend on } i_p.$$

Above three constants may be determined from any one set of characteristic curves.

$$r_p = \frac{V_{P1} - V_{P2}}{I_{PA} - I_{PB}},$$

$$g_m = \frac{I_{PA} - I_{PB}}{V_{G1} - V_{G2}},$$

$$\mu = -\frac{V_{P1} - V_{P2}}{V_{G2} - V_{G1}}$$

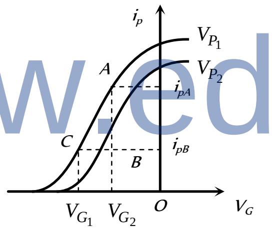


Fig. 27.79

Triode as an Amplifiers

Amplifier is a device by which the amplitude of variation of *ac* signal voltage / current/ power can be increased

(1) The signal to be amplified (V_i) is applied in the grid circuit and amplified output is obtained from the plate circuit

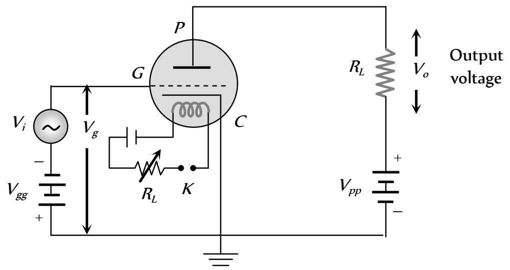


Fig. 27.80

(2) The voltage at grid is the sum of signal V_i and grid bias V_{gg}.

$$V_g = V_{gg} + V_i$$

(3) Small change in grid voltage results in a large change in plate current so results in a large change in voltage across $R_L\ (V_0 = i_p R_L \Rightarrow \Delta V_0 = \Delta i_p R_L)$

(4) The linear portion of the mutual characteristic with maximum slope is chosen for amplification without distortion.

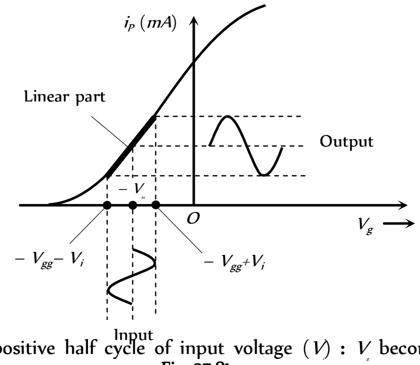


Fig. 27.81

(i) For the positive half cycle of input voltage (V_i) : V_g becomes less negative, so i_p increases

(ii) For the negative half cycle of input voltage (V_i) : V_g becomes more negative, so i_p decreases

(iii) The phase difference between the output signal and input signal is 180° (or π)

(5) **Voltage amplification**

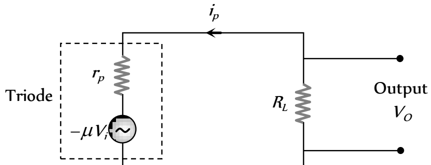


Fig. 27. 82 : Equivalent circuit of triode amplifier

Current through the load resistance is given by $i_p = -\frac{\mu V_i}{r_p + R_L}$

$$\Rightarrow V_0 = i_p R_L = \frac{-\mu V_i R_L}{r_p + R_L} \Rightarrow \text{Voltage gain} = \frac{V_0}{V_i} = -\frac{\mu R_L}{r_p + R_L}$$

$$\text{Numerically } A = \frac{\mu R_L}{r_p + R_L} = \frac{\mu}{1 + \frac{r_p}{R_L}}$$

(i) If $R_L = \infty \Rightarrow A$ will be maximum and $A_{max} = \mu$

(Practically $A < \mu$)

(ii) If $r_p = R_L \Rightarrow A = \frac{\mu}{2}$

(iii) Power at load resistance $P = i_p V_0 = i_p^2 R_L$

Condition for maximum power $R_L = r_p$

$$\therefore P_{max} = \left(\frac{\mu V_i}{R_L + R_L}\right)^2 \times R_L = \frac{\mu^2 V_i^2}{4 R_L}$$

Tips & Tricks

✍ The most efficient packing of atoms in cubic lattice structure occurs for *fcc*.

- The lattice for *NaCl* crystal is *fcc*.

- The space lattice of diamond is *fcc*. (The diamond structure may be viewed as two *fcc* structures displaced from each other by one quarter of a body diagonal).

- Carbon, silicon, germanium, tin can crystallize in the diamond structure.

- At room temperature $\sigma_{Ge} > \sigma_{Si}$

- $(n_i)_{Ge} \simeq 2.4 \times 10^{19} / m^3$ and $(n_i)_{Si} \simeq 1.5 \times 10^{16} / m^3$

- In a transistor circuit the reverse bias is high as compared to the forward bias. So that it may exert a large attractive force on the charge carriers to enter the collector region.

- *Ge* is more sensitive to heat since it's forbidden energy gap is smaller than that of silicon. Electrons from the valence band of *Ge* requires less energy to move from the valence band to conduction band.

- Both *N*-type as well as *P*-type semiconductor are neutral.

- Semiconductor devices are current control devices.

- The semiconductor devices are temperature sensitive devices.

- The electric field setup across the potential barrier is of the order of 3×10^5 *V/m* for *Ge* and 7×10^5 *V/m* for *Si*.

- An ideal junction diode when forward biased offers zero resistance. Voltage drop across such a junction diode is zero. In reverse biased diode offers infinite resistance and voltage drop across it is equal to voltage applied.

- A *P-N* junction diode can be considered to be equivalent to a capacitor with *P* and *N* regions acting as the plates of the capacitors and depletion layer as the dielectric medium.

- The mobility of electron is two-three times the mobility of holes. Therefore NPN devices are fast and hence preferred.

- If $E_g \simeq 0\,eV$, the material is good conductor or metal and if $E_g \simeq 1\,eV$, the material is a semiconductor. If $E_g \simeq 6\,eV$ then the material is an insulator.

- A *P-N* junction or diode acts like a valve or voltage controlled switch. When forward biased, it acts like ON switch. When reverse biased, it acts like an OFF switch.

- The current due to minority carriers in the junction diode is independent of the applied voltage. It only depends upon the temperature of the diode.

- Voltage obtained from a diode rectifier is a mixture of alternating and direct voltage.

- Cross sectional area of base is very large as compared to emitter. Cross sectional area of collector is less than base but greater than emitter.

- C.C (common collector) amplifier is called power amplifier or current booster or emitter follower.

- Devices like tunnel diode, tetrode and thyrisisters have negative resistance.

- Transistor provides good power amplification when they are use in CE configuration.

- **MOSFETS :** In a MOSFET, a type of three-terminal transistor, a potential applied to the gate terminal *G* controls the internal flow of electrons from the source terminal *S* to the drain terminal *D*. Commonly, a MOSFET is operated only in its ON (conducting) or OFF (not conducting condition. Installed by the thousands and millions on silicon wafers (chips) to form integrated circuits, MOSFETs form the basis for computer hardware.

- When a *PN* junction is forward biased, it can emit light, hence can serve as a light-emitting diode (LED). The wavelength of the emitted light is $\lambda = \frac{c}{f} = \frac{hc}{E_g}$

- The fermi energy of a given material is the energy of a quantum state that has the probability 0.5 of being occupied by an electron.

- Number of conduction electrons per unit volume

$$= \frac{\text{(Material's density)}}{\text{(Molar mass } M)/N_A}$$

(N_A = Avogadro's number = 6.02×10^{23} */mol*)

- The occupancy probability $P(E)$: Electrical conduction of a metal depends on the probability that if an energy level is available at energy *E*, is it actually occupied by an electron.

the expression for occupancy probability $P(E)$ is given by

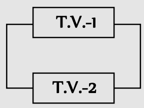
Fermi-Dirac statistics $P(E) = \dfrac{1}{\exp\left(\dfrac{E - E_F}{kT}\right) + 1}$; E_F=Fermi energy

- A good emitter should have low work function, high melting point, high working temperature, high electrical and mechanical strength.

- When triode amplifier are in series, total voltage gain

$A = A_1 A_2 A_3$ ....

- When two triode valve are in parallel



Total plate resistance $\frac{1}{r_p} = \frac{1}{r_{p_1}} + \frac{1}{r_{p_2}}$

Total mutual conductance $G_m = g_{m_1} + g_{m_2}$

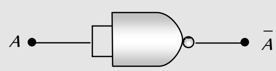
Total amplification factor $\mu = G_m R_p$

Voltage amplification $A = \frac{\mu R_L}{r_p + R_L}$

- **NOR** gate is a universal gate because it can be used to perform the basic logic function, AND, OR and NOT.

- Output in Ex-OR gate is '1' only when inputs are different.

- If both inputs of NAND gate are shorted then it will become 'NOT gate



NOT gate

Ordinary Thinking

Objective Questions

Solids and Crystals

1. The nature of binding for a crystal with alternate and evenly spaced positive and negative ions is [CBSE PMT 2000]
   (a) Covalent (b) Metallic
   (c) Dipolar (d) Ionic

2. For a crystal system, $a = b = c$, $\alpha = \beta = \gamma \neq 90^\circ$, the system is [BHU 2000]
   (a) Tetragonal system (b) Cubic system
   (c) Orthorhombic system (d) Rhombohedral system

3. Biaxial crystal among the following is [Pb. CET 1998]
   (a) Calcite (b) Quartz
   (c) Selenite (d) Tourmaline

4. The temperature coefficient of resistance of a conductor is [AFMC 1998]
   (a) Positive always (b) Negative always
   (c) Zero (d) Infinite

5. Potassium has a *bcc* structure with nearest neighbour distance 4.525 Å. Its molecular weight is 39. Its density in kg/m is [DCE 1997]
   (a) 900 (b) 494
   (c) 602 (d) 802

6. The expected energy of the electrons at absolute zero is called [RPET 1996]
   (a) Fermi energy (b) Emission energy
   (c) Work function (d) Potential energy

7. In a triclinic crystal system [EAMCET (Med.) 1995]
   (a) $a \neq b \neq c$, $\alpha \neq \beta \neq \gamma$ (b) $a = b = c$, $\alpha \neq \beta \neq \gamma$
   (c) $a \neq b \neq c$, $\alpha \neq \beta = \gamma$ (d) $a = b \neq c$, $\alpha = \beta = \gamma$

8. Metallic solids are always opaque because [AFMC 1994]
   (a) Solids effect the incident light
   (b) Incident light is readily absorbed by the free electron in a metal
   (c) Incident light is scattered by solid molecules
   (d) Energy band traps the incident light

9. In which of the following ionic bond is present [EAMCET (Med.) 1994]
   (a) $NaCl$ (b) Ar
   (c) Si (d) Ge

10. Which of the following materials is non crystalline [CBSE PMT 1993]
    (a) Copper (b) Sodium chloride
    (c) Wood (d) Diamond

11. The coordination number of Cu is [AMU 1992]

(a) 1 (b) 6

(c) 8 (d) 12

12. Which one of the following is the weakest kind of bonding in solids[CBSE PMT 1992; KCET 1992]

(a) Ionic (b) Metallic

(c) Vander Waals (d) Covalent

13. In a crystal, the atoms are located at the position of [AMU 1985]

(a) Maximum potential energy

(b) Minimum potential energy

(c) Zero potential energy

(d) Infinite potential energy

14. Crystal structure of $NaCl$ is [NCERT 1982]

(a) Fcc (b) Bcc

(c) Both of the above (d) None of the above

15. What is the coordination number of sodium ions in the case of sodium chloride structure [CBSE PMT 1988]

(a) 6 (b) 8

(c) 4 (d) 12

16. The distance between the body centred atom and a corner atom in sodium (a = 4.225 Å) is [CBSE PMT 1995]

(a) 3.66 Å (b) 3.17 Å

(c) 2.99 Å (d) 2.54 Å

17. A solid that transmits light in visible region and has a very low melting point possesses [J & K CET 2001]

(a) Metallic bonding (b) Ionic bonding

(c) Covalent bonding (d) Vander Waal's bonding

18. Atomic radius of *fcc* is [J & K CET 2001]

(a) $\frac{a}{2}$ (b) $\frac{a}{2\sqrt{2}}$

(c) $\frac{\sqrt{3}}{4}a$ (d) $\frac{\sqrt{3}}{2}a$

19. A solid reflects incident light and it's electrical conductivity decreases with temperature. The binding in this solids

(a) Ionic (b) Covalent

(c) Metallic (d) Molecular

20. The laptop PC's modern electronic watches and calculators use the following for display

(a) Single crystal (b) Poly crystal

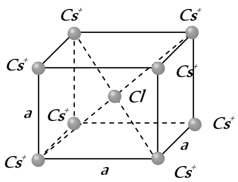
(c) Liquid crystal (d) Semiconductors

21. The nearest distance between two atoms in case of a bcc lattice is equal to [J & K CET 2004]

(a) $a\frac{\sqrt{2}}{3}$ (b) $a\frac{\sqrt{3}}{2}$

(c) $q\sqrt{3}$ (d) $\frac{a}{\sqrt{2}}$

22. What is the net force on a Cl placed at the centre of the *bcc* structure of $CsCl$ [DCE 2003; AIIMS 2004]



(a) Zero (b) ke^2/a^2

(c) ke^2a^2 (d) Data is incomplete

23. Sodium has body centred packing. If the distance between two nearest atoms is 3.7 Å, then its lattice parameter is [Pb. PET 2002]

(a) 4.8 Å (b) 4.3 Å

(c) 3.9 Å (d) 3.3 Å

24. Which of the following is an amorphous solid [AIIMS 2005; J & K CET 2004]

(a) Glass (b) Diamond

(c) Salt (d) Sugar

25. Copper has face centered cubic (*fcc*) lattice with interatomic spacing equal to 2.54Å. The value of the lattice constant for this lattice is

(a) 1.27 Å (b) 5.08 Å

(c) 2.54 Å (d) 3.59 Å

26. In good conductors of electricity, the type of bonding that exists is

(a) Ionic (b) Vander Waals

(c) Covalent (d) Metallic

27. Bonding in a germanium crystal (semi- conductor) is [CPMT 1986; KCET 1992; EAMCET (Med.) 1995; MP PET/PMT 2004]

(a) Metallic (b) Ionic

(c) Vander Waal's type (d) Covalent

28. The ionic bond is absent in [J & K CET 2005]

(a) $NaCl$ (b) $CsCl$

(c) LiF (d) H_2O

Semiconductors

1. The majority charge carriers in P-type semiconductor are [MP PMT 1999; CBSE PMT 1999; MP PET 1991; MP PET/PMT 1998; MH CET 2003]

(a) Electrons (b) Protons

(c) Holes (d) Neutrons

2. A P-type semiconductor can be obtained by adding [NCERT 1979; BIT 1988; MP PMT 1987; 90]

(a) Arsenic to pure silicon

(b) Gallium to pure silicon

(c) Antimony to pure germanium

(d) Phosphorous to pure germanium

3. The valence of an impurity added to germanium crystal in order to convert it into a P-type semi conductor is [MP PMT 1989; CPMT 1987]

(a) 6 (b) 5

(c) 4 (d) 3

4. In a semiconductor, the concentration of electrons is $8\times10^{14}/cm^3$ and that of the holes is $5\times10^{12}cm^3$. The semiconductor is [MP PMT 1997; RPET 1999; Kerala PET 2002]

(a) *P*-type (b) *N*-type

(c) Intrinsic (d) *PNP*-type

5. In *P*-type semiconductor, there is [MP PMT 1989]

(a) An excess of one electron

(b) Absence of one electron

(c) A missing atom

(d) A donar level

6. The valence of the impurity atom that is to be added to germanium crystal so as to make it a *N*-type semiconductor, is

[MNR 1993; MP PET 1994; CBSE PMT 1999; AIIMS 2000]

(a) 6 (b) 5

(c) 4 (d) 3

7. Silicon is a semiconductor. If a small amount of *As* is added to it, then its electrical conductivity [MP PMT 1996]

(a) Decreases (b) Increases

(c) Remains unchanged (d) Becomes zero

8. When the electrical conductivity of a semi- conductor is due to the breaking of its covalent bonds, then the semiconductor is said to be

[AIIMS 1997; KCET (Engg.) 2002]

(a) Donar (b) Acceptor

(c) Intrinsic (d) Extrinsic

9. A piece of copper and the other of germanium are cooled from the room temperature to 80 K, then which of the following would be a correct statement

[IIT-JEE 1988; Bihar CEE 1992; CBSE PMT 1993; MP PET 1997; RPET 1999; AIEEE 2004]

(a) Resistance of each increases

(b) Resistance of each decreases

(c) Resistance of copper increases while that of germanium decreases

(d) Resistance of copper decreases while that of germanium increases

10. To obtain *P*-type Si semiconductor, we need to dope pure Si with [IIT-JEE 1988; MP PET 1997, 93; Pb. PMT 2001, 02; UPSEAT 2004]

(a) Aluminium (b) Phosphorous

(c) Oxygen (d) Germanium

11. Electrical conductivity of a semiconductor

[MP PMT 1993, 2000; RPET 1996]

(a) Decreases with the rise in its temperature

(b) Increases with the rise in its temperature

(c) Does not change with the rise in its temperature

(d) First increases and then decreases with the rise in its temperature

12. Three semi-conductors are arranged in the increasing order of their energy gap as follows. The correct arrangement is

[MP PMT 1993]

(a) Tellurium, germanium, silicon

(b) Tellurium, silicon, germanium

(c) Silicon, germanium, tellurium

(d) Silicon, tellurium, germanium

13. When a semiconductor is heated, its resistance

[KCET 1992; MP PMT 1994; MP PET 1992, 2002; RPMT 2001; DCE 2001]

(a) Decreases (b) Increases

(c) Remains unchanged (d) Nothing is definite

14. In an insulator, the forbidden energy gap between the valence band and conduction band is of the order of

[DPMT 1988; EAMCET (Engg.) 1995; MP PET 1996]

(a) $1\,MeV$ (b) $0.1\,MeV$

(c) $1\,eV$ (d) $5\,eV$

15. A *N*-type semiconductor is [AFMC 1988; RPMT 1999]

(a) Negatively charged (b) Positively charged

(c) Neutral (d) None of these

16. The energy band gap of Si is

[MP PET 1994, 2002; BHU 1995; RPMT 2000]

(a) $0.70\,eV$

(b) 1.1 eV

(c) Between $0.70\,eV$ to $1.1\,eV$

(d) 5 eV

17. The forbidden energy band gap in conductors, semiconductors and insulators are EG_1, EG_2 and EG_3 respectively. The relation among them is

[MP PMT 1994; RPMT 1997]

(a) $EG_1 = EG_2 = EG_3$ (b) $EG_1 < EG_2 < EG_3$

(c) $EG_1 > EG_2 > EG_3$ (d) $EG_1 < EG_2 > EG_3$

18. Which statement is correct [MP PMT 1994]

(a) *N*-type germanium is negatively charged and *P*-type germanium is positively charged

(b) Both *N*-type and *P*-type germanium are neutral

(c) *N*-type germanium is positively charged and *P*-type germanium is negatively charged

(d) Both *N*-type and *P*-type germanium are negatively charged

19. When *Ge* crystals are doped with phosphorus atom, then it becomes [AFMC 1995; Orissa PMT 2004]

(a) Insulator (b) *P*-type

(c) *N*-type (d) Superconductor

20. Let n_P and n_e be the number of holes and conduction electrons respectively in a semiconductor. Then

[MP PET 1995]

(a) $n_P > n_e$ in an intrinsic semiconductor

(b) $n_P = n_e$ in an extrinsic semiconductor

(c) $n_P = n_e$ in an intrinsic semiconductor

(d) $n_e > n_P$ in an intrinsic semiconductor

21. Wires P and Q have the same resistance at ordinary (room) temperature. When heated, resistance of P increases and that of Q decreases. We conclude that [MP PMT 1995; MP PET 2001]

(a) P and Q are conductors of different materials

(b) P is N-type semiconductor and Q is P-type semiconductor

(c) P is semiconductor and Q is conductor

(d) P is conductor and Q is semiconductor

22. The impurity atoms which are mixed with pure silicon to make a P-type semiconductor are those of [MP PMT 1995]

(a) Phosphorus (b) Boron

(c) Antimony (d) Copper

23. Holes are charge carriers in [IIT-JEE 1996]

(a) Intrinsic semiconductors (b) Ionic solids

(c) P-type semiconductors (d) Metals

24. In extrinsic P and N-type, semiconductor materials, the ratio of the impurity atoms to the pure semiconductor atoms is about

(a) 1 (b) 10^{-1}

(c) 10^{-4} (d) 10^{-7}

25. A hole in a P-type semiconductor is [MP PET 1996]

(a) An excess electron (b) A missing electron

(c) A missing atom (d) A donor level

26. The forbidden gap in the energy bands of germanium at room temperature is about [MP PMT/PET 1998]

(a) $1.1 eV$ (b) $0.1 eV$

(c) $0.67 eV$ (d) $6.7 eV$

27. In P-type semiconductor the majority and minority charge carriers are respectively [EAMCET 1994; MP PMT/PET 1998; MH CET 2000]

(a) Protons and electrons (b) Electrons and protons

(c) Electrons and holes (d) Holes and electrons

28. At zero Kelvin a piece of germanium [MP PET 1999]

(a) Becomes semiconductor

(b) Becomes good conductor

(c) Becomes bad conductor

(d) Has maximum conductivity

29. Electronic configuration of germanium is 2, 8, 18 and 4. To make it extrinsic semiconductor small quantity of antimony is added

(a) The material obtained will be N-type germanium in which electrons and holes are equal in number

(b) The material obtained will be P-type germanium

(c) The material obtained will be N-type germanium which has more electrons than holes at room temperature

(d) The material obtained will be N-type germanium which has less electrons than holes at room temperature

30. A semiconductor is cooled from $T_1 K$ to $T_2 K$. Its resistance [MP PET 1999]

(a) Will decrease

(b) Will increase

(c) Will first decrease and then increase

(d) Will not change

31. If N_P and N_e be the numbers of holes and conduction electrons in an extrinsic semiconductor, then [MP PMT 1999; AMU 2001]

(a) $N_P > N_e$

(b) $N_P = N_e$

(c) $N_P < N_e$

(d) $N_P > N_e$ or $N_P < N_e$ depending on the nature of impurity

32. In intrinsic semiconductor at room temperature, number of electrons and holes are [EAMCET (Engg.) 1995; JIPMER 2001, 02]

(a) Equal (b) Zero

(c) Unequal (d) Infinite

33. (USS 133) Indium impurity in germanium makes [EAMCET (Engg.) 1995] [MP PET 2003]

(a) N-type (b) P-type

(c) Insulator (d) Intrinsic

34. Fermi level of energy of an intrinsic semiconductor lies [EAMCET (Med.) 1995]

(a) In the middle of forbidden gap

(b) Below the middle of forbidden gap

(c) Above the middle of forbidden gap

(d) Outside the forbidden gap

35. In a semiconductor the separation between conduction band and valence band is of the order of [EAMCET (Med.) 1995; AIIMS 2000]

(a) $100 eV$ (b) $10 eV$

(c) $1 eV$ (d) 0 eV

36. The intrinsic semiconductor becomes an insulator at [EAMCET (Med.) 1995; KCET (Engg./Med.) 1999; MP PET 2000; CBSE PMT 2001]

(a) $0°C$ (b) $-100°C$

(c) $300 K$ (d) $0 K$

37. The addition of antimony atoms to a sample of intrinsic germanium transforms it to a material which is [AMU 1995] [MP PET 1999]

(a) Superconductor (b) An insulator

(c) N-type semiconductor (d) P-type semiconductor

38. Resistance of semiconductor at $0°K$ is [RPET 1997]

(a) Zero (b) Infinite

(c) Large (d) Small

39. In a good conductor the energy gap between the conduction band and the valence band is [KCET 1993; EMCET (Med.) 1994]

(a) Infinite (b) Wide

(c) Narrow (d) Zero

40. The impurity atom added to germanium to make it N-type semiconductor is [KCET 1993; KCET (Engg./Med.) 2000]

(a) Arsenic (b) Iridium
(c) Aluminium (d) Iodine

41. When N-type of semiconductor is heated [CBSE PMT 1993; DPMT 2000]
(a) Number of electrons increases while that of holes decreases
(b) Number of holes increases while that of electrons decreases
(c) Number of electrons and holes remains same
(d) Number of electrons and holes increases equally

42. To obtain a P-type germanium semiconductor, it must be doped with [CBSE PMT 1997; Pb. PET 2000]
(a) Arsenic (b) Antimony
(c) Indium (d) Phosphorus

43. The temperature coefficient of resistance of a semiconductor [AFMC 1998, MNR 1998]
(a) Is always positive
(b) Is always negative
(c) Is zero
(d) May be positive or negative or zero

44. P-type semiconductor is formed when [RPET 1999]
A. As impurity is mixed in Si
B. Al impurity is mixed in Si
C. B impurity is mixed in Ge
D. P impurity is mixed in Ge
(a) A and C (b) A and D
(c) B and C (d) B and D

45. In case of a semiconductor, which of the following statement is wrong [Pb. PMT 1999]
(a) Doping increases conductivity
(b) Temperature coefficient of resistance is negative
(c) Resisitivity is in between that of a conductor and insulator
(d) At absolute zero temperature, it behaves like a conductor

46. Energy bands in solids are a consequence of [DCE 1999, 2000; AIEEE 2004]
(a) Ohm's Law
(b) Pauli's exclusion principle
(c) Bohr's theory
(d) Heisenberg's uncertainty principle

47. In a P-type semiconductor [AIIMS 1997; Orissa JEE 2002; MP PET 2003]
(a) Current is mainly carried by holes
(b) Current is mainly carried by electrons
(c) The material is always positively charged
(d) Doping is done by pentavalent material

48. At ordinary temperatures, the electrical conductivity of semi conductors in $mho/meter$ is in the range [MP PET 2003]
(a) 10^{-3} to 10^{-4} (b) 10^{6} to 10^{9}
(c) 10^{-6} to 10^{-10} (d) 10^{-10} to 10^{-16}

49. When the temperature of silicon sample is increased from $27°C$ to $100°C$, the conductivity of silicon will be [RPMT 1999]
(a) Increased (b) Decreased
(c) Remain same (d) Zero

50. In a P-type semiconductor, germanium is doped with [AFMC 1999]
(a) Boron (b) Gallium
(c) Aluminium (d) All of these

51. In N-type semiconductors, majority charge carriers are [AIIMS 1999]
(a) Holes (b) Protons
(c) Neutrons (d) Electrons

52. Semiconductor is damaged by the strong current due to [MH CET 2000]
(a) Lack of free electron (b) Excess of electrons
(c) Excess of proton (d) None of these

53. GaAs is [RPMT 2000]
(a) Element semiconductor
(b) Alloy semiconductor
(c) Bad conductor
(d) Metallic semiconductor

54. If n_e and n_h are the number of electrons and holes in a semiconductor heavily doped with phosphorus, then [MP PMT 2000]
(a) $n_e >> n_h$ (b) $n_e << n_h$
(c) $n_e \le n_h$ (d) $n_e = n_h$

55. An N-type and P-type silicon can be obtained by doping pure silicon with [EAMCET (Med.) 2000]
(a) Arsenic and Phosphorous (b) Indium and Aluminium
(c) Phosphorous and Indium (d) Aluminium and Boron

56. N-type semiconductors will be obtained, when germanium is doped with [AIIMS 2000]
(a) Phosphorus (b) Aluminium
(c) Arsenic (d) Both (a) or (c)

57. The state of the energy gained by valance electrons when the temperature is raised or when electric field is applied is called as
(a) Valance band (b) Conduction band
(c) Forbidden band (d) None of these

58. To obtain electrons as majority charge carriers in a semiconductor, the impurity mixed is [MP PET 2000]
(a) Monovalent (b) Divalent
(c) Trivalent (d) Pentavalent

59. For germanium crystal, the forbidden energy gap in joules is [MP PET 2000]
(a) 1.12×10^{-19} (b) 1.76×10^{-19}
(c) 1.6×10^{-19} (d) Zero

60. A pure semiconductor behaves slightly as a conductor at [MH CET (Med.) 2001; BHU 2000; AFMC 2001]
(a) Room temperature (b) Low temperature

(c) High temperature (d) Both (b) and (c)

61. Which is the correct relation for forbidden energy gap in conductor, semi conductor and insulator [RPMT 2001; AIEEE 2002]

(a) $\Delta Eg_c > \Delta Eg_{sc} > \Delta Eg_{\text{insulator}}$

(b) $\Delta Eg_{\text{insulator}} > \Delta Eg_{sc} > \Delta Eg_{\text{conductor}}$

(c) $\Delta Eg_{\text{conductor}} > \Delta Eg_{\text{insulator}} > \Delta Eg_{sc}$

(d) $\Delta Eg_{sc} > \Delta Eg_{\text{conductor}} > \Delta Eg_{\text{insulator}}$

62. The band gap in Germanium and silicon in eV respectively is

(a) 0.7, 1.1 (b) 1.1, 0.7

(c) 1.1, 0 (d) 0, 1.1

63. P-type semiconductors are made by adding impurity element

(a) As (b) P

(c) B (d) Bi

64. At room temperature, a P-type semiconductor has [Kerala PMT 2002]

(a) Large number of holes and few electrons

(b) Large number of free electrons and few holes

(c) Equal number of free electrons and holes

(d) No electrons or holes

65. In intrinsic semiconductor at room temperature, number of electrons and holes are [JIPMER 2001, 02; MP PMT 2002]

(a) Unequal (b) Equal

(c) Infinite (d) Zero

66. The valence band and conduction band of a solid overlap at low temperature, the solid may be [Orissa JEE 2002; BCECE 2004]

(a) A metal (b) A semiconductor

(c) An insulator (d) None of these

67. Which impurity is doped in Si to form N-type semi-conductor? [CBSE PMT 1996; AIEEE 2002]

(a) Al (b) B

(c) As (d) None of these

68. In a semiconductor [AIEEE 2002; AIIMS 2002]

(a) There are no free electrons at any temperature

(b) The number of free electrons is more than that in a conductor

(c) There are no free electrons at 0 K

(d) None of these

69. The energy band gap is maximum in [AIEEE 2002]

(a) Metals (b) Superconductors

(c) Insulators (d) Semiconductors

70. The process of adding impurities to the pure semiconductor is called [MH CET 2002]

(a) Drouping (b) Drooping

(c) Doping (d) None of these

71. When phosphorus and antimony are mixed in zermaniun, then

(a) P-type semiconductor is formed

(b) N-type semiconductor is formed

(c) Both (a) and (b)

(d) None of these

72. To a germanium sample, traces of gallium are added as an impurity. The resultant sample would behave like [AIIMS 2003]

(a) A conductor

(b) A P-type semiconductor

(c) An N-type semiconductor

(d) An insulator [MP PMT 2001]

73. For non-conductors, the energy gap is [EAMCET (Engg.) 1995; MP PET 1996; RPET 2003]

(a) 6 eV [MP PMT 2001] (b) 1.1 eV

(c) 0.8 eV (d) 0.3 eV

74. Donor type impurity is found in [RPET 2003]

(a) Trivalent elements (b) Pentavalent elements

(c) In both the above (d) None of these

75. The difference in the variation of resistance with temperature in a metal and a semiconductor arises essentially due to the difference in the [AIEEE 2003]

(a) Variation of scattering mechanism with temperature

(b) Crystal structure

(c) Variation of the number of charge carriers with temperature

(d) Type of bon

76. The charge on a hole is equal to the charge of [MP PMT 2004]

(a) Zero (b) Proton

(c) Neutron (d) Electron

77. When germanium is doped with phosphorus, the doped material has

(a) Excess positive charge

(b) Excess negative charge

(c) More negative current carriers

(d) More positive current carriers

78. A Ge specimen is doped with Al. The concentration of acceptor atoms is ~10^{21} $atoms/m^3$. Given that the intrinsic concentration of electron hole pairs is $\sim 10^{19}/m^3$, the concentration of electrons in the specimen is [AIIMS 2004]

(a) $10^{17}/m^3$ (b) $10^{15}/m^3$

(c) $10^4/m^3$ (d) $10^2/m^3$

79. Which of the following has negative temperature coefficient of resistance [AFMC 2004]

(a) Copper (b) Aluminium

(c) Iron (d) Germanium

80. In semiconductors at a room temperature [CPMT 2003] [CBSE PMT 2004]

(a) The valence band is partially empty and the conduction band is partially filled

(b) The valence band is completely filled and the conduction band is partially filled

(c) The valence band is completely filled

(d) The conduction band is completely empty

81. Regarding a semiconductor which one of the following is wrong

(a) There are no free electrons at room temperature

(b) There are no free electrons at 0 K

(c) The number of free electrons increases with rise of temperature

(d) The charge carriers are electrons and holes

82. Which of the following statements is true for an N-type semi-conductor [CPMT 2004]

(a) The donor level lies closely below the bottom of the conduction band

(b) The donor level lies closely above the top of the valence band

(c) The donor level lies at the halfway mark of the forbidden energy gap

(d) None of above

83. Choose the correct statement [DCE 2004]

(a) When we heat a semiconductor its resistance increases

(b) When we heat a semiconductor its resistance decreases

(c) When we cool a semiconductor to 0 K then it becomes super conductor

(d) Resistance of a semiconductor is independent of temperature

84. In a P-type semi-conductor, germanium is dopped with [MH CET 2003]

(a) Gallium (b) Boron

(c) Aluminium (d) All of these

85. A piece of semiconductor is connected in series in an electric circuit. On increasing the temperature, the current in the circuit will

(a) Decrease (b) Remain unchanged

(c) Increase (d) Stop flowing

86. Intrinsic semiconductor is electrically neutral. Extrinsic semiconductor having large number of current carriers would be

(a) Positively charged

(b) Negatively charged

(c) Positively charged or negatively charged depending upon the type of impurity that has been added

(d) Electrically neutral

87. If n and v be the number of electrons and drift velocity in a semiconductor. When the temperature is increased [Pb. CET 2000]

(a) n increases and v decreases

(b) n decreases and v increases

(c) Both n and v increases

(d) Both n and v decreases

88. In extrinsic semiconductors [EAMCET (Engg.) 1999]

(a) The conduction band and valence band overlap

(b) The gap between conduction band and valence band is more than 16 eV

(c) The gap between conduction band and valence band is near about 1 eV

(d) The gap between conduction band and valence band will be 100 eV and more [CPMT 2004]

89. Resistivity of a semiconductor depends on [MP PMT 1999]

(a) Shape of semiconductor

(b) Atomic nature of semiconductor

(c) Length of semiconductor

(d) Shape and atomic nature of semiconductor

90. Electric current is due to drift of electrons in [CPMT 1996]

(a) Metallic conductors

(b) Semi-conductors

(c) Both (a) and (b)

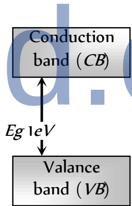
(d) None of these

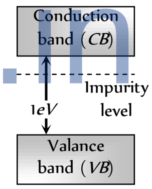
91. The energy gap of silicon is 1.14 eV. The maximum wavelength at which silicon will begin absorbing energy is [MP PMT 1993]

(a) 10888 $Å$ (b) 1088.8 $Å$

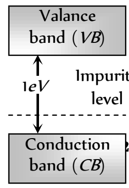
(c) 108.88 $Å$ (d) 10.888 $Å$

92. Which of the following energy band diagram shows the N-type semiconductor [RPET 1986]

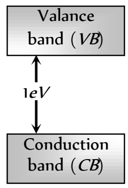
(a)


(b)


[RPMT 2003]

(c)


2001]

(d)


93. The mobility of free electron is greater than that of free holes because

(a) The carry negative charge

(b) They are light

(c) They mutually collide less

(d) They require low energy to continue their motion

94. The relation between the number of free electrons in semiconductors (n) and its temperature (T) is

(a) $n \propto T^2$ (b) $n \propto T$

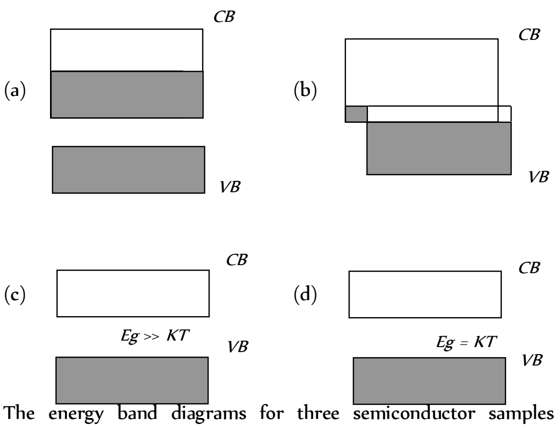
(c) $n \propto \sqrt{T}$ (d) $n \propto T^{3/2}$

95. The electron mobility in *N*-type germanium is 3900 *cm/v-s* and its conductivity is 6.24 *mho/cm*, then impurity concentration will be if the effect of cotters is negligible

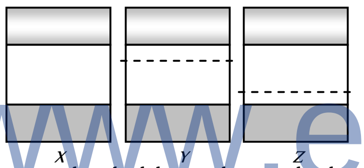
(a) 10^{15} cm^{3} (b) 10^{13} $/cm^{3}$

(c) 10^{12} $/cm^{3}$ (d) 10^{16} $/cm^{3}$

96. Which of the energy band diagrams shown in the figure corresponds to that of a semiconductor [Orissa JEE 2003]



97. The energy band diagrams for three semiconductor samples of silicon are as shown. We can then assert that [Haryana CEE 1996]



(a) Sample *X* is undoped while samples *Y* and *Z* have been doped with a third group and a fifth group impurity respectively

(b) Sample *X* is undoped while both samples *Y* and *Z* have been doped with a fifth group impurity

(c) Sample *X* has been doped with equal amounts of third and fifth group impurities while samples *Y* and *Z* are undoped

(d) Sample *X* is undoped while samples *Y* and *Z* have been doped with a fifth group and a third group impurity respectively

98. Carbon, silicon and Germanium atoms have four valence electrons each. Their valence and conduction band are separated by energy band gaps represented by $(E_g)_C$. $(E_g)_{Si}$ and $(E_g)_{Ge}$ respectively. Which one of the following relationship is true in their case

(a) $(E_g)_C > (E_g)_{Si}$ (b) $(E_g)_C = (E_g)_{Si}$

(c) $(E_g)_C < (E_g)_{Ge}$ (d) $(E_g)_C < (E_g)_{Si}$

99. A semiconductor dopped with a donor impurity is [AFMC 2005]

(a) *P*-type (b) *N*-type

(c) *NPN* type (d) *PNP* type

100. In a semiconducting material the mobilities of electrons and holes are μ_e and μ_h respectively. Which of the following is true

(a) $\mu_e > \mu_h$ (b) $\mu_e < \mu_h$

(c) $\mu_e = \mu_h$ (d) $\mu_e < 0; \mu_h > 0$

101. Doping of intrinsic semiconductor is done [Orissa JEE 2005]

(a) To neutralize charge carriers

(b) To increase the concentration of majority charge carriers

(c) To make it neutral before disposal

(d) To carry out further purification

Semiconductor Diode

1. In the forward bias arrangement of a *PN*-junction diode [MP PMT 1994, 96, 99]

(a) The *N*-end is connected to the positive terminal of the battery

(b) The *P*-end is connected to the positive terminal of the battery

(c) The direction of current is from *N*-end to *P*-end in the diode

(d) The *P*-end is connected to the negative terminal of battery

2. In a *PN*-junction diode [MP PET 1993]

(a) The current in the reverse biased condition is generally very small

(b) The current in the reverse biased condition is small but the forward biased current is independent of the bias voltage

(c) The reverse biased current is strongly dependent on the applied bias voltage

(d) The forward biased current is very small in comparison to reverse biased current

3. The cut-in voltage for silicon diode is approximately

(a) 0.2 V (b) 0.6 V

(c) 1.1 V (d) 1.4 V

4. The electrical circuit used to get smooth *dc* output from a rectifier circuit is called [KCET 2003]

(a) Oscillator (b) Filter

(c) Amplifier (d) Logic gates

5. *PN*-junction diode works as a insulator, if connected [CPMT 1987]

(a) To A.C. (b) In forward bias

(c) In reverse bias (d) None of these

6. The reverse biasing in a *PN* junction diode [MP PMT 1991; EAMCET 1994; CBSE PMT 2003]

(a) Decreases the potential barrier

(b) Increases the potential barrier

(c) Increases the number of minority charge carriers

[CBSE PMT 2005]

(d) Increases the number of majority charge carriers

7. The electrical resistance of depletion layer is large because

(a) It has no charge carriers

(b) It has a large number of charge carriers

(c) It contains electrons as charge carriers

(d) It has holes as charge carriers

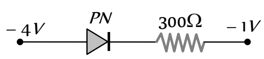
8. In the circuit given below, the value of the current is

[AIIMS 2005]

(a) 0 *amp* (b) 10^{-2} *amp*

(c) 10^{2} *amp* (d) 10^{-3} *amp*

9. What is the current in the circuit shown below [AFMC 2000; RPMT 2001]



(a) 0 *amp* (b) 10^{-2} *amp*

(c) 1 *amp* (d) 0.10 *amp*

10. If the forward voltage in a semiconductor diode is doubled, the width of the depletion layer will [MP PMT 1996]

(a) Become half (b) Become one-fourth

(c) Remain unchanged (d) Become double

11. The *PN* junction diode is used as [CPMT 1972; AFMC 1997; CBSE PMT 1999; AIIMS 1999; RPMT 2000; MP PMT 04]

(a) An amplifier (b) A rectifier

(c) An oscillator (d) A modulator

12. When a *PN* junction diode is reverse biased

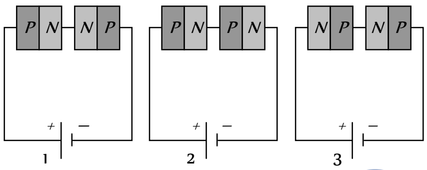
(a) Electrons and holes are attracted towards each other and move towards the depletion region

(b) Electrons and holes move away from the junction depletion region

(c) Height of the potential barrier decreases

(d) No change in the current takes place

13. Two *PN*-junctions can be connected in series by three different methods as shown in the figure. If the potential difference in the junctions is the same, then the correct connections will be



(a) In the circuit (1) and (2) (b) In the circuit (2) and (3)

(c) In the circuit (1) and (3) (d) Only in the circuit (1)

14. A *PN*- junction has a thickness of the order of [BIT 1990]

(a) $1\,cm$ (b) $1\,mm$

(c) $10^{-6}\,m$ (d) $10^{-12}\,cm$

15. In the depletion region of an unbiased *P-N* junction diode there are [KCET 1999; CBSE PMT 1999; RPMT 2001; MP PMT 1994, 2003]

(a) Only electrons

(b) Only holes

(c) Both electrons and holes

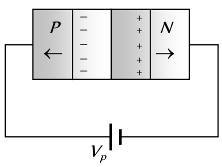
(d) Only fixed ions

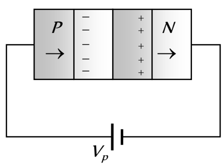
16. On increasing the reverse bias to a large value in a *PN*-junction diode, current [MP PMT 1994; BHU 2002]

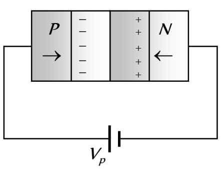
(a) Increases slowly (b) Remains fixed

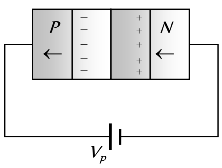
(c) Suddenly increases (d) Decreases slowly

17. In the case of forward biasing of *PN*-junction, which one of the following figures correctly depicts the direction of flow of carriers

(a) 

(b) 

(c) 

(d) 

18. Which of the following statements concerning the depletion zone of an unbiased *PN* junction is (are) true [IIT-JEE 1995]

(a) The width of the zone is independent of the densities of the dopants (impurities)

(b) The width of the zone is dependent on the densities of the dopants

(c) The electric field in the zone is produced by the ionized dopant atoms

(d) The electric field in the zone is provided by the electrons in the conduction band and the holes in the valence band

19. A semiconductor device is connected in a series circuit with a battery and a resistance. A current is found to pass through the circuit. If the polarity of the battery is reversed, the current drops almost to zero. The device may be [MP PET 1995; CBSE PMT 1998]

(a) A *P*-type semiconductor (b) An *N*-type semiconductor

(c) A *PN*-junction [IIT-JEE 1989] (d) An intrinsic semiconductor

20. The approximate ratio of resistances in the forward and reverse bias of the *PN*-junction diode is [MP PET 2000; MP PMT 1999, 2002, 03; Pb. PMT 2003]

(a) $10^2 : 1$ (b) $10^{-2} : 1$

(c) $1 : 10^{-4}$ (d) $1 : 10^4$

21. In a junction diode, the holes are due to [CBSE PMT 1999; Pb. PMT 2003]

(a) Protons (b) Neutrons

(c) Extra electrons (d) Missing of electrons

22. In forward bias, the width of potential barrier in a *P-N* junction diode [EAMCET (Engg.) 1995; CBSE PMT 1999 RPMT 1997, 2002, 03]

(a) Increases

(b) Decreases

(c) Remains constant

(d) First increases then decreases

23. The cause of the potential barrier in a *P-N* diode is [CBSE PMT 1998; RPMT 2001]

(a) Depletion of positive charges near the junction

(b) Concentration of positive charges near the junction

(c) Depletion of negative charges near the junction

(d) Concentration of positive and negative charges near the junction

24. In a *PN*-junction diode [CBSE PMT 1998] not connected to any circuit [IIT-JEE 1998]

(a) The potential is the same everywhere

(b) The *P*-type is a higher potential than the *N*-type side

(c) There is an electric field at the junction directed from the *N*-type side to the *P*- type side

(d) There is an electric field at the junction directed from the *P*-type side to the *N*-type side

25. Which of the following statements is not true [IIT-JEE 1997 Re-Exam]

(a) The resistance of intrinsic semiconductors decrease with increase of temperature

(b) Doping pure *Si* with trivalent impurities give *P*-type semiconductors

(c) The majority carriers in *N*-type semiconductors are holes

(d) A *PN*-junction can act as a semiconductor diode

26. The dominant mechanisms for motion of charge carriers in forward and reverse biased silicon *P*-*N* junctions are [IIT-JEE 1997 Cancelled; RPMT 2000; AIIMS 2000]

(a) Drift in forward bias, diffusion in reverse bias

(b) Diffusion in forward bias, drift in reverse bias

(c) Diffusion in both forward and reverse bias

(d) Drift in both forward and reverse bias

27. In *P*-*N* junction, avalanche current flows in circuit when biasing is

(a) Forward (b) Reverse

(c) Zero (d) Excess

28. The depletion layer in the *P*-*N* junction region is caused by [CBSE PMT 1994]

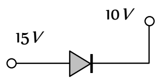
(a) Drift of holes

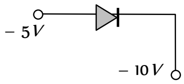
(b) Diffusion of charge carriers

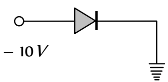
(c) Migration of impurity ions

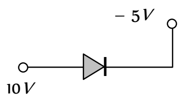
(d) Drift of electrons

29. Which one is reverse-biased [DCE 1999]

(a) 

(b) 

(c) 

(d) 

30. In a *P*-*N* junction diode if *P* region is heavily doped than *n* region then the depletion layer is [RPMT 1999]

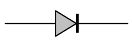
(a) Greater in *P* region

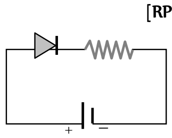
(b) Greater in *N* region

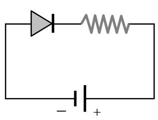
(c) Equal in both region

(d) No depletion layer is formed in this case

31. Which one is in forward bias [RPMT 2000]

(a) 

(b) 

(c) 

(d) None of these

32. The reason of current flow in *P*-*N* junction in forward bias is [RPMT 2000]

(a) Drifting of charge carriers

(b) Minority charge carriers

(c) Diffusion of charge carriers

(d) All of these

33. The resistance of a reverse biased *P*-*N* junction diode is about

(a) 1 *ohm* (b) 10^2 *ohm*

(c) 10^3 *ohm* (d) 10^6 *ohm*

34. Consider the following statements *A* and *B* and identify the correct choice of the given answers

A: The width of the depletion layer in a *P*-*N* junction diode increases in forwards bias

B: In an intrinsic semiconductor the fermi energy level is exactly in the middle of the forbidden gap [EAMCET (Engg.) 2000]

(a) *A* is true and *B* is false (b) Both *A* and *B* are false

(c) *A* is false and *B* is true (d) Both *A* and *B* are true

[RPET 1997]

35. In comparison to a half wave rectifier, the full wave rectifier gives lower [AFMC 2001]

(a) Efficiency (b) Average *dc*

(c) Average output voltage (d) None of these

36. Avalanche breakdown is due to [RPMT 2001]

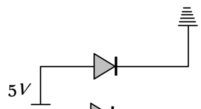
(a) Collision of minority charge carrier

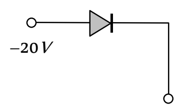
(b) Increase in depletion layer thickness

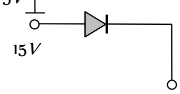
(c) Decrease in depletion layer thickness

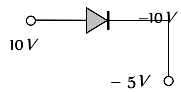
(d) None of these

37. Which is reverse biased diode [DCE 2001]

(a) 

(b) 

(c) 

(d) 

38. Zener breakdown in a semi-conductor diode occurs when [UPSEAT 2002]

(a) Forward current exceeds certain value

(b) Reverse bias exceeds certain value

(c) Forward bias exceeds certain value

(d) Potential barrier is reduced to zero

39. When forward bias is applied to a *P*-*N* junction, then what happens to the potential barrier V_B, and the width of charge depleted region *x* [UPSEAT 2002, 03; Roorkee 1999; RPET 2003; AIEEE 2004]

(a) V_B increases, *x* decreases

(b) V_B decreases, *x* increases

(c) V_B increases, *x* increases

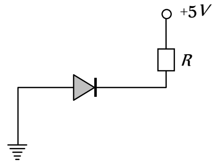
(d) V_B decreases, *x* decreases

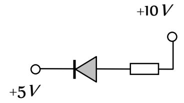
40. The potential barrier, in the depletion layer, is due to [EAMCET (Engg.) 1998; Pb. PMT 1999; Pb. PET 2001; AIIMS 2002]

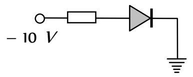
(a) Ions (b) Holes

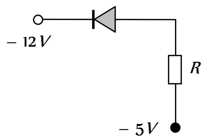
(c) Electrons (d) Both (b) and (c)

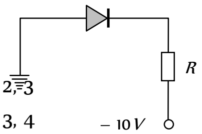
41. In the given figure, which of the diodes are forward biased ? [Kerala PET 2002]

1. 

2. 

3. 

4. 

5. 

(a) 1, 2, 3 (b) 2, 4, 5

(c) 1, 3, 4 (d) 2, 3, 4

42. Function of rectifier is [AFMC 2002, 04]

(a) To convert *ac* into *dc* (b) To convert *dc* into *ac*

(c) Both (a) and (b) (d) None of these

43. When the *P* end of *P-N* junction is connected to the negative terminal of the battery and the *N* end to the positive terminal of the battery, then the *P-N* junction behaves like

(a) A conductor (b) An insulator

(c) A super-conductor (d) A semi-conductor

44. If the two ends *P* and *N* of a *P-N* diode junction are joined by a wire [MP PMT 2002]

(a) There will not be a steady current in the circuit

(b) There will be a steady current from *N* side to *P* side

(c) There will be a steady current from *P* side to *N* side

(d) There may not be a current depending upon the resistance of the connecting wire

45. A potential barrier of 0.50 *V* exists across a *P-N* junction. If the depletion region is 5.0×10^{-7} *m* wide, the intensity of the electric field in this region is [UPSEAT 2002]

(a) 1.0×10^{6} *V/m* (b) 1.0×10^{5} *V/m*

(c) 2.0×10^{5} *V/m* (d) 2.0×10^{6} *V/m*

46. If no external voltage is applied across *P-N* junction, there would be

(a) No electric field across the junction

(b) An electric field pointing from *N*-type to *P*-type side across the junction

(c) An electric field pointing from *P*-type to *N*-type side across the junction

(d) A temporary electric field during formation of *P-N* junction that would subsequently disappear

47. In a *PN*-junction [CBSE PMT 2002]

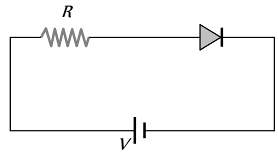
(a) *P* and *N* both are at same potential

(b) High potential at *N* side and low potential at *P* side

(c) High potential at *P* side and low potential at *N* side

(d) Low potential at *N* side and zero potential at *P* side

48. For the given circuit of *PN*-junction diode, which of the following statement is correct [CBSE PMT 2002]



(a) In forward biasing the voltage across *R* is *V*

(b) In forward biasing the voltage across *R* is 2*V*

(c) In reverse biasing the voltage across *R* is *V*

(d) In reverse biasing the voltage across *R* is 2*V*

49. On adjusting the *P-N* junction diode in forward biased [RPET 2003]

(a) Depletion layer increases (b) Resistance increases

(c) Both decreases (d) None of these

50. In the middle of the depletion layer of a reverse-biased *PN* junction, the [AIEEE 2003]

(a) Potential is zero (b) Electric field is zero

(c) Potential is maximum (d) Electric field is maximum

51. Barrier potential of a *P-N* junction diode does not depend on

(a) Temperature (b) Forward bias

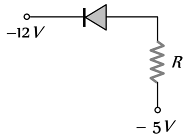
(c) Doping density [MP PET 2002] (d) Diode design

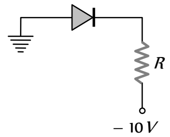
52. A crystal diode is a [MP PET 2004]

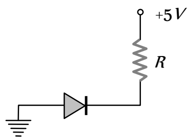
(a) Non-linear device (b) Amplifying device

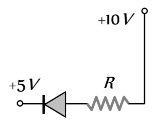
(c) Linear device (d) Fluctuating device

53. Of the diodes shown in the following diagrams, which one is reverse biased [CBSE PMT 2004]

(a) 

(b) 

(c) 

(d) 

54. In a *PN*-junction photo cell, the value of photo-electromotive force produced by monochromatic light is proportional to [Orissa JEE 2002] [CBSE PMT 2004]

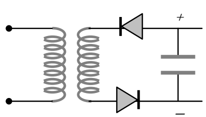
(a) The voltage applied at the *PN* junction

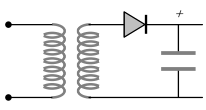
(b) The barrier voltage at the *PN* junction

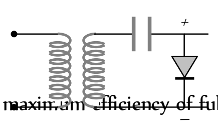
(c) The intensity of the light falling on the cell

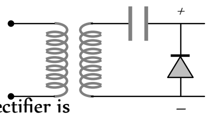
(d) The frequency of the light falling on the cell

55. Which is the correct diagram of a half-wave rectifier [Orissa PMT 2004]

(a) 

(b) 

(c) 

(d) 

56. The maximum efficiency of full wave rectifier is [J & K CET 2004]

(a) 100% (b) 25.20%

(c) 40.2% (d) 81.2%

57. Serious draw back of the semiconductor device is [Pb. PMT 2004]

(a) They cannot be used with high voltage

(b) They pollute the environment

(c) They are costly

(d) They do not last for long time

58. Select the correct statement [RPMT 2003]

(a) In a full wave rectifier, two diodes work alternately

(b) In a full wave rectifier, two diodes work simultaneously

(c) The efficiency of full wave and half wave rectifiers is same

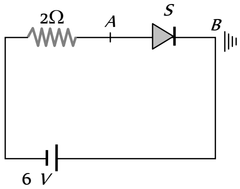
(d) The full wave rectifier is bi-directional.

59. In order to forward bias a *PN* junction, the negative terminal of battery is connected to [RPMT 2003]

(a) *P*-side (b) Either *P*-side or *N*-side

(c) *N*-side (d) None of these

60. The diode shown in the circuit is a silicon diode. The potential difference between the points *A* and *B* will be [RPMT 2002]



(a) 6 *V*

(b) 0.6 *V*

(c) 0.7 *V*

(d) 0 *V*

61. Zener breakdown takes place if [RPMT 2000]

(a) Doped impurity is low (b) Doped impurity is high

(c) Less impurity in *N*-part (d) Less impurity in *P*-type

62. Consider the following statements *A* and *B* and identify the correct choice of the given answers

(A) A zener diode is always connected in reverse bias

(B) The potential barrier of a *PN* junction lies between 0.1 to 0.3 *V* approximately [EAMCET 2000]

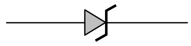
(a) *A* and *B* are correct

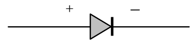
(b) *A* and *B* are wrong

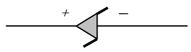
(c) *A* is correct but *B* is wrong

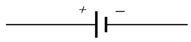
(d) *A* is wrong but *B* is correct

63. The correct symbol for zener diode is [RPMT 2000]

(a) 

(b) 

(c) 

(d) 

64. Which one of the following statements is not correct [SCRA 2000]

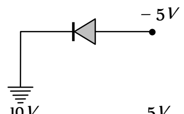
(a) A diode does not obey Ohm's law

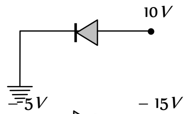
(b) A *PN* junction diode symbol shows an arrow identifying the direction of current (forward) flow

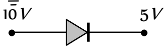
(c) An ideal diode is an open switch

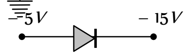
(d) An ideal diode is an ideal one way conductor

65. Which of the following semi-conductor diodes is reverse biased

(a) 

(b) 

(c) 

(d) 

66. No bias is applied to a *P-N* junction, then the current [RPMT 1999]

(a) Is zero because the number of charge carriers flowing on both sides is same

(b) Is zero because the charge carriers do not move

(c) Is non-zero

(d) None of these

67. Zener diode is used as [CBSE PMT 1999]

(a) Half wave rectifier (b) Full wave rectifier

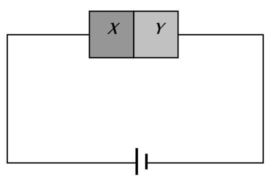
(c) ac voltage stabilizer (d) dc voltage stabilizer

68. The width of forbidden gap in silicon crystal is 1.1 *eV*. When the crystal is converted in to a *N*-type semiconductor the distance of Fermi level from conduction band is [EAMCET (Med.) 1999]

(a) Greater than 0.55 *eV* (b) Equal to 0.55 *eV*

(c) Lesser than 0.55 *eV* (d) Equal to 1.1 *eV*

69. A semiconductor *X* is made by doping a germanium crystal with arsenic (Z = 33). A second semiconductor *Y* is made by doping germanium with indium (Z = 49). The two are joined end to end and connected to a battery as shown. Which of the following statements is correct [Orissa JEE 1998]



(a) *X* is *P*-type, *Y* is *N*-type and the junction is forward biased

(b) *X* is *N*-type, *Y* is *P*-type and the junction is forward biased

(c) *X* is *P*-type, *Y* is *N*-type and the junction is reverse biased

(d) *X* is *N*-type, *Y* is *P*-type and the junction is reverse biased

70. In *P-N* junction, the barrier potential offers resistance to [AMU 1995, 96]

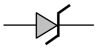
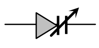
(a) Free electrons in *N* region and holes in *P* region

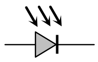
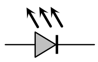
(b) Free electrons in *P* region and holes in *N* region

(c) Only free electrons in *N* region

(d) Only holes in *P* region

71. Symbolic representation of photodiode is [RPMT 1995]

(a)  (b) 

(c)  (d) 

72. To make a *PN* junction conducting [IIT-JEE 1994]

(a) The value of forward bias should be more than the barrier potential

(b) The value of forward bias should be less than the barrier potential

(c) The value of reverse bias should be more than the barrier potential

(d) The value of reverse bias should be less than the barrier potential

73. Which is the wrong statement in following sentences? A device in which *P* and *N*-type semiconductors are used is more useful then a vacuum type because [MP PET 1992]

(a) Power is not necessary to heat the filament

(b) It is more stable

(c) Very less heat is produced in it

(d) Its efficiency is high due to a high voltage across the junction

74. The depletion layer in silicon diode is 1 μm wide and the knee potential is 0.6 *V*, then the electric field in the depletion layer will be

(a) Zero

(b) 0.6 Vm^{-1}

(c) 6×10^4 V/m

(d) 6×10^5 V/m

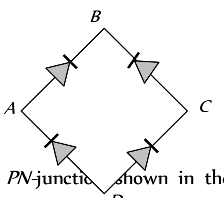
75. In the diagram, the input is across the terminals *A* and *C* and the output is across the terminals *B* and *D*, then the output is

(a) Zero

(b) Same as input

(c) Full wave rectifier

(d) Half wave rectifier



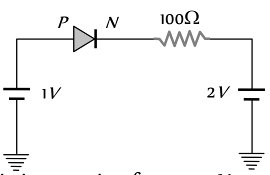
76. The current through an ideal *PN*-junction shown in the following circuit diagram will be [AMU 1998]

(a) Zero

(b) 1 *mA*

(c) 10 *mA*

(d) 30 *mA*



77. If a full wave rectifier circuit is operating from 50 *Hz* mains, the fundamental frequency in the ripple will be

[UPSEAT 2000; CBSE PMT 2003; AIEEE 2005]

(a) 50 *Hz* (b) 70.7 *Hz*

(c) 100 *Hz* (d) 25 *Hz*

78. In a full wave rectifiers, input *ac* current has a frequency '*ν*'. The output frequency of current is [BHU 2005]

(a) *ν*/2 (b) *ν*

(c) 2*ν* (d) None of these

79. A diode having potential difference 0.5 *V* across its junction which does not depend on current, is connected in series with resistance of 20 Ω across source. If 0.1 *A* passes through resistance then what is the voltage of the source

[DCE 2005]

(a) 1.5 *V* (b) 2.0 *V*

(c) 2.5 *V* (d) 5 *V*

Junction Transistor

1. When *NPN* transistor is used as an amplifier

[AIEEE 2004]

(a) Electrons move from base to collector

(b) Holes move from emitter to base

(c) Electrons move from collector to base

(d) Holes move from base to emitter

2. The phase difference between input and output voltages of a CE circuit is [MP PET 2004]

(a) 0° (b) 90°

(c) 180° (d) 270°

3. An oscillator is nothing but an amplifier with

[MP PET 2004]

(a) Positive feed back (b) Large gain

(c) No feedback (d) Negative feedback

4. The emitter-base junction of a transistor is ...... biased while the collector-base junction is .... biased

[CBSE PMT 1994] [KCET 2004]

(a) Reverse, forward (b) Reverse, reverse

(c) Forward, forward (d) Forward, reverse

5. In an *NPN* transistor the collector current is 24 *mA*. If 80% of electrons reach collector its base current in *mA* is

[Kerala PMT 2004]

(a) 36 (b) 26

(c) 16 (d) 6

6. A *NPN* transistor conducts when [CPMT 2003]

(a) Both collector and emitter are positive with respect to the base

(b) Collector is positive and emitter is negative with respect to the base

(c) Collector is positive and emitter is at same potential as the base

(d) Both collector and emitter are negative with respect to the base

7. In the case of constants α and β of a transistor [CET 2003]

(a) $\alpha = \beta$ (b) $\beta < 1 \quad \alpha > 1$

(c) $\alpha\beta = 1$ (d) $\beta > 1 \quad \alpha < 1$

8. Which of the following is true [DPMT 2002]

(a) Common base transistor is commonly used because current gain is maximum

(b) Common emitter is commonly used because current gain is maximum

(c) Common collector is commonly used because current gain is maximum

(d) Common emitter is the least used transistor

9. If $\alpha = 0.98$ and current through emitter $i_e = 20$ mA, the value of β is [DPMT 2002]

(a) 4.9 (b) 49

(c) 96 (d) 9.6

10. For a common base configuration of PNP transistor $\frac{I_C}{I_E} = 0.98$ then maximum current gain in common emitter configuration will be [CBSE PMT 2002]

(a) 12 (b) 24

(c) 6 (d) 5

11. In a PNP transistor working as a common-base amplifier, current gain is 0.96 and emitter current is 7.2 mA. The base current is [AFMC 2002; Pb. PET 2002]

(a) 0.4 mA (b) 0.2 mA

(c) 0.29 mA (d) 0.35 mA

12. If l_1, l_2, l_3 are the lengths of the emitter, base and collector of a transistor then [KCET 2002]

(a) $l_1 = l_2 = l_3$ (b) $l_3 < l_2 > l_1$

(c) $l_3 < l_1 < l_2$ (d) $l_3 > l_1 > l_2$

13. In an NPN transistor circuit, the collector current is 10 mA. If 90% of the electrons emitted reach the collector, the emitter current (i_E) and base current (i_B) are given by [KCET 2001]

(a) $i_E = -1$ mA, $i_B = 9$ mA

(b) $i_E = 9$ mA, $i_B = -1$ mA

(c) $i_E = 1$ mA, $i_B = 11$ mA

(d) $i_E = 11$ mA, $i_B = 1$ mA

14. In a common emitter transistor, the current gain is 80. What is the change in collector current, when the change in base current is 250 μA [CBSE PMT 2000]

(a) 80×250 μA (b) $(250 - 80)$ μA

(c) $(250 + 80)$ μA (d) 250/80 μA

15. Least doped region in a transistor [KCET 2000]

(a) Either emitter or collector

(b) Base

(c) Emitter

(d) Collector

16. The transistors provide good power amplification when they are used in [AMU 1999]

(a) Common collector configuration

(b) Common emitter configuration

(c) Common base configuration

(d) None of these

17. The transfer ratio of a transistor is 50. The input resistance of the transistor when used in the common-emitter configuration is 1 $K\Omega$. The peak value for an A.C input voltage of 0.01 V peak is

(a) 100 μA (b) 0.01 mA

(c) 0.25 mA (d) 500 μA

18. For a transistor the parameter $\beta = 99$. The value of the parameter α is [Pb CET 1998]

(a) 0.9 (b) 0.99

(c) 1 (d) 9

19. A transistor is used in common emitter mode as an amplifier. Then

(a) The base-emitter junction is forward biased

(b) The base-emitter junction is reverse biased

(c) The input signal is connected in series with the voltage applied to the base-emitter junction

(d) The input signal is connected in series with the voltage applied to bias the base collector junction

20. In a PNP transistor the base is the N-region. Its width relative to the P-region is [DCE 1997]

(a) Smaller (b) Larger

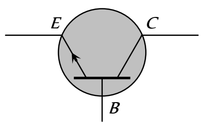
(c) Same (d) Not related

21. A common emitter amplifier is designed with NPN transistor ($\alpha = 0.99$). The input impedance is 1 $K\Omega$ and load is 10 $K\Omega$. The voltage gain will be [CPMT 1996]

(a) 9.9 (b) 99

(c) 990 (d) 9900

22. The symbol given in figure represents [AMU 1995, 96]



(a) NPN transistor

(b) PNP transistor

(c) Forward biased PN junction diode

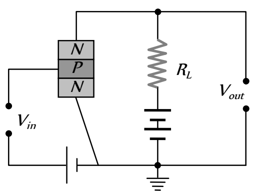
(d) Reverse biased NP junction diode

23. The most commonly used material for making transistor is [MNR 1995]

(a) Copper (b) Silicon

(c) Ebonite (d) Silver

24. An NPN-transistor circuit is arranged as shown in figure. It is [BHU 1994]



(a) A common base amplifier circuit

(b) A common emitter amplifier circuit

(c) A common collector amplifier circuit

(d) Neither of the above

25. The part of a transistor which is heavily doped to produce a large number of majority carriers, is [CBSE PMT 1993]

(a) Base (b) Emitter

(c) Collector (d) None of these

26. For a transistor, the current amplification factor is 0.8. The transistor is connected in common emitter configuration. The change in the collector current when the base current changes by 6 *mA* is [Haryana CET 1991]

(a) 6 *mA* (b) 4.8 *mA*

(c) 24 *mA* (d) 8 *mA*

27. In a common base amplifier circuit, calculate the change in base current if that in the emitter current is 2 *mA* and α = 0.98

[BHU 1995]

(a) 0.04 *mA* (b) 1.96 *mA*

(c) 0.98 *mA* (d) 2 *mA*

28. In case of *NPN*-transistors the collector current is always less than the emitter current because [AIIMS 1983]

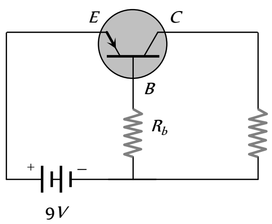
(a) Collector side is reverse biased and emitter side is forward biased

(b) After electrons are lost in the base and only remaining ones reach the collector

(c) Collector side is forward biased and emitter side is reverse biased

(d) Collector being reverse biased attracts less electrons

29. In a transistor circuit shown here the base current is 35 μA. The value of the resistor R_b is



(a) 123.5 $k\Omega$

(b) 257 $k\Omega$

(c) 380.05 $k\Omega$

(d) None of these

30. In a transistor, a change of 8.0 *mA* in the emitter current produces a change of 7.8 *mA* in the collector current. What change in the base current is necessary to produce the same change in the collector current

(a) 50 μA (b) 100 μA

(c) 150 μA (d) 200 μA

31. In a transistor configuration β-parameter is

[Orissa PMT 2004]

(a) $\frac{I_b}{I_c}$ (b) $\frac{I_c}{I_b}$

(c) $\frac{I_c}{I_a}$ (d) $\frac{I_a}{I_c}$

32. Which of these is unipolar transistor [Pb PMT 2004]

(a) Point contact transistor (b) Field effect transistor

(c) *PNP* transistor (d) None of these

33. For a transistor, in a common emitter arrangement, the alternating current gain β is given by [DPMT 2004]

(a) $\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_C}$ (b) $\beta = \left(\frac{\Delta I_B}{\Delta I_C}\right)_{V_C}$

(c) $\beta = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_C}$ (d) $\beta = \left(\frac{\Delta I_E}{\Delta I_C}\right)_{V_C}$

34. The relation between α and β parameters of current gains for a transistors is given by [Pb. PET 2000]

(a) $\alpha = \frac{\beta}{1-\beta}$ (b) $\alpha = \frac{\beta}{1+\beta}$

(c) $\alpha = \frac{1-\beta}{\beta}$ (d) $\alpha = \frac{1+\beta}{\beta}$

35. When *NPN* transistor is used as an amplifier [DCE 2002]

(a) Electrons move from base to emitter

(b) Electrons move from emitter to base

(c) Electrons moves from base to emitter

(d) Holes moves from base to emitter

36. In the *CB* mode of a transistor, when the collector voltage is changed by 0.5 *volt*. The collector current changes by 0.05 *mA*. The output resistance will be [Pb. PMT 2003]

(a) 10 $k\Omega$ (b) 20 $k\Omega$

(c) 5 $k\Omega$ (d) 2.5 $k\Omega$

37. Which of the following is used to produce radio waves of constant amplitude [DCE 2004]

(a) Oscillator (b) FET

(c) Rectifier (d) Amplifier

38. While a collector to emitter voltage is constant in a transistor, the collector current changes by 8.2 *mA* when the emitter current changes by 8.3 *mA*. The value of forward current ratio h_{fe} is

(a) 82 (b) 83

(c) 8.2 (d) 8.3

39. Consider an *NPN* transistor amplifier in common-emitter configuration. The current gain of the transistor is 100. If the collector current changes by 1 *mA*, what will be the change in emitter current [AIIMS 2005]

(a) 1.1 *mA* (b) 1.01 *mA*

(c) 0.01 *mA* (d) 10 *mA*

40. In a common base amplifier the phase difference between the input signal voltage and the output voltage is

[CBSE PMT 1990; AIEEE 2005]

(a) 0 (b) $\pi / 4$

(c) $\pi / 2$ (d) π

41. In *NPN* transistor the collector current is 10 *mA*. If 90% of electrons emitted reach the collector, then [Kerala PMT 2005]

(a) Emitter current will be 9 *mA*

(b) Emitter current will be 11.1 *mA*

(c) Base current will be 0.1 *mA*

(d) Base current will be 0.01 *mA*

42. *NPN* transistor are preferred to *PNP* transistor because they have [J & K CET 2005]

(a) Low cost

(b) Low dissipation energy

(c) Capability of handing large power

(d) Electrons having high mobility than holes

43. In a transistor in CE configuration, the ratio of power gain to voltage gain is [J & K CET 2005]

(a) α (b) β / α

(c) $\beta\alpha$ (d) β

44. In the study of transistor as an amplifier, if $\alpha = I_c / I_e$ and $\beta = I_c / I_b$, where I_c, I_b and I_e are the collector, base and emitter currents, then

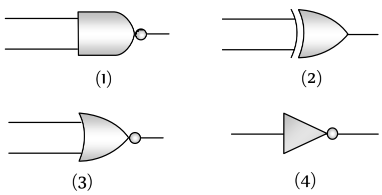
[CBSE PMT 2000; KCET 2000; Orissa JEE 2005]

(a) $\beta = \frac{1-\alpha}{\alpha}$ (b) $\beta = \frac{\alpha}{1-\alpha}$

(c) $\beta = \frac{\alpha}{1+\alpha}$ (d) $\beta = \frac{1+\alpha}{\alpha}$

Digital Electronics

1. Given below are symbols for some logic gates

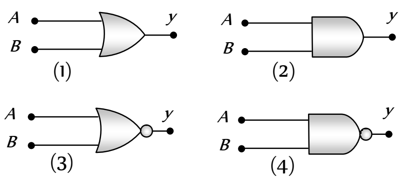


The XOR gate and NOR gate respectively are [AFMC 1994]

(a) 1 and 2 (b) 2 and 3

(c) 3 and 4 (d) 1 and 4

2. Given below are four logic gate symbol (figure). Those for OR, NOR and NAND are respectively [NSEP 1994]



(a) 1, 4, 3 (b) 4, 1, 2

(c) 1, 3, 4 (d) 4, 2, 1

3. The following truth table corresponds to the logic gate

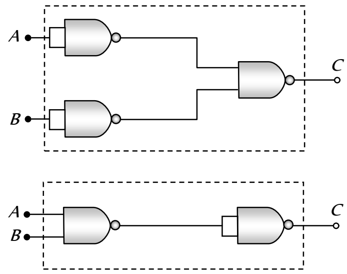
[BHU 1994; CPMT 2000; J & K CET 2004]

A	0	0	1	1
B	0	1	0	1
X	0	1	1	1

(a) NAND (b) OR

(c) AND (d) XOR

4. The combination of 'NAND' gates shown here under (figure) are equivalent to [Haryana CEET 1996]



(a) An OR gate and an AND gate respectively

(b) An AND gate and a NOT gate respectively

(c) An AND gate and an OR gate respectively

(d) An OR gate and a NOT gate respectively.

5. A truth table is given below. Which of the following has this type of truth table [CBSE PMT 1996; UPSEAT 2002]

A	0	1	0	1
B	0	0	1	1
y	1	0	0	0

(a) XOR gate (b) NOR gate

(c) AND gate (d) OR gate

6. The truth table shown in figure is for [Pb. CET 1998]

A	0	0	1	1
B	0	1	0	1
Y	1	0	0	1

(a) XOR (b) AND

(c) XNOR (d) OR

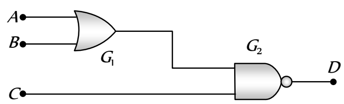
7. For the given combination of gates, if the logic states of inputs *A*, *B*, *C* are as follows *A* = *B* = *C* = 0 and *A* = *B* = 1, *C* = 0 then the logic states of output *D* are

(a) 0, 0

(b) 0, 1

(c) 1, 0

(d) 1, 1



8. Boolean algebra is essentially based on [AIIMS 1999]

(a) Truth (b) Logic

(c) Symbol (d) Numbers

9. The logic behind 'NOR' gate is that it gives

[CPMT 1999, AFMC 1999]

(a) High output when both the inputs are low

(b) Low output when both the inputs are low

(c) High output when both the inputs are high

(d) None of these

10. A logic gate is an electronic circuit which [BHU 2000]

(a) Makes logic decisions

(b) Allows electrons flow only in one direction

(c) Works binary algebra

(d) Alternates between 0 and 1 values

11. A gate has the following truth table [CBSE PMT 2000]

P	1	1	0	0
Q	1	0	1	0
R	1	0	0	0

The gate is

(a) NOR (b) OR

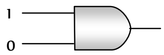
(c) NAND (d) AND

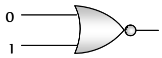
12. How many NAND gates are used to form an AND gate [MP PET 2004]

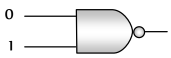
(a) 1 (b) 2

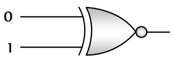
(c) 3 (d) 4

13. Which of the following gates will have an output of 1 [CBSE PMT 1998]

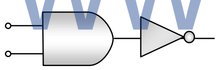
(a) 

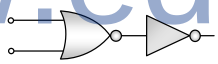
(b) 

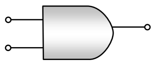
(c) 

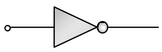
(d) 

14. Which represents NAND gate [DCE 2002]

(a) 

(b) 

(c) 

(d) 

15. The given truth table is of [AMU 1998; J & K CET 2002]

A	X
0	1
1	0

(a) OR gate (b) AND gate

(c) NOT gate (d) None of above

16. What will be the input of A and B for the Boolean expression $\overline{(A+B)}\cdot\overline{(A\cdot B)}=1$ [TNPCEE 2002]

(a) 0, 0 (b) 0, 1

(c) 1, 0 (d) 1, 1

17. If A and B are two inputs in AND gate, then AND gate has an output of 1 when the values of A and B are [TNPCEE 2002]

(a) $A = 0,\ B = 0$ (b) $A = 1,\ B = 1$

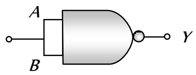
(c) $A = 1,\ B = 0$ (d) $A = 0,\ B = 1$

18. The Boolean equation of NOR gate is [Haryana CET 2002]

(a) $C = A + B$ (b) $C = \overline{A+B}$

(c) $C = A \cdot B$ (d) $C = \overline{A \cdot B}$

19. This symbol represents [CBSE PMT 1996]



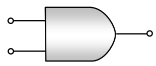
(a) NOT gate

(b) OR gate

(c) AND gate

(d) NOR gate

20. Which logic gate is represented by following diagram [DCE 2001]

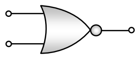


(a) AND

(b) OR

(c) NOR

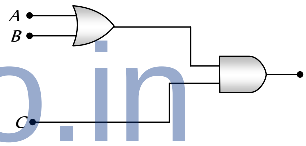
(d) XOR

21. Symbol  represents [Kerala PMT 2001]

(a) NAND gate (b) NOR gate

(c) NOT gate (d) XNOR gate

22. To get an output 1 from the circuit shown in the figure, the input must be [UPSEAT 2002]



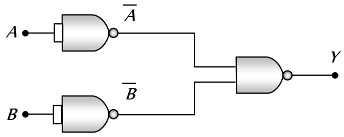
(a) $A=0,\ B=1,\ C=0$

(b) $A=1,\ B=0,\ C=0$

(c) $A=1,\ B=0,\ C=1$

(d) $A=1,\ B=1,\ C=0$

23. The combination of the gates shown in the figure below produces



(a) NOR gate

(b) OR gate

(c) AND gate

(d) XOR gate

24. The output of a NAND gate is 0 [UPSEAT 2004]

(a) If both inputs are 0

(b) If one input is 0 and the other input is 1

(c) If both inputs are 1

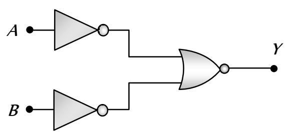
(d) Either if both inputs are 1 or if one of the inputs is 1 and the other 0

25. A gate in which all the inputs must be low to get a high output is called [UPSEAT 2004]

(a) A NAND gate (b) An inverter

(c) A NOR gate (d) An AND gate

26. Which logic gate is represented by the following combination of logic gates [AIIMS 2004]



(a) OR (b) NAND

(c) AND (d) NOR

27. The output of OR gate is 1 [CBSE PMT 2004]

(a) If both inputs are zero

(b) If either or both inputs are 1

(c) Only if both input are 1

(d) If either input is zero

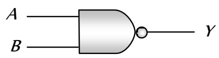
28. Which gates is represented by this figure [DCE 2003]

(a) NAND gate

(b) AND gate

(c) NOT gate

(d) OR gate



29. Sum of the two binary numbers $(1000010)_2$ and $(11011)_2$ is

(a) $(111101)_2$ (b) $(111111)_2$

(c) $(101111)_2$ (d) $(111001)_2$

30. The truth-table given below is for which gate

[CBSE PMT 1994, 98 2002; DPMT 2002; BCECE 2005]

A	0	0	1	1
B	0	1	0	1
C	1	1	1	0

(a) XOR (b) OR

(c) AND (d) NAND

31. Which of the following logic gate is an universal gate

[AIIMS 2005]

(a) OR (b) NOT

(c) AND (d) NOR

Valve Electronics (Diode and Triode)

1. Thermionic emission from a heated filament varies with its temperature T as

[CBSE PMT 1990; RPMT 2000; CPMT 2002]

(a) T^{-1} (b) T

(c) T^2 (d) $T^{3/2}$

2. Number of secondary electrons emitted per number of primary electrons depends on [RPET 2000]

(a) Material of target

(b) Frequency of primary electrons

(c) Intensity

(d) None of the above

3. Due to S.C.R in vacuum tube [RPET 2000]

(a) $I_p \rightarrow$ Decrease (b) $I_p -$ Increase

(c) $V_p =$ Increase (d) $V_g =$ Increase

4. In diode, when there is saturation current, the plate resistance (r_p) is [AIIMS 1997; Haryana PMT 2000]

(a) Zero (b) Infinite

(c) Some finite quantity (d) Data is insufficient

5. The grid voltage of any triode valve is changed from –1 volt to – 3 *volt* and the mutual conductance is 3×10^{-4} *mho*. The change in plate circuit current will be [MNR 1999]

(a) 0.8 *mA* (b) 0.6 *mA*

(c) 0.4 *mA* (d) 1 *mA*

6. In a triode, $g_m = 2 \times 10^{-3} ohm^{-1}; \mu = 42$, resistance load, $R = 50$ kilo ohm. The voltage amplification obtained from this triode will be [MNR 1999]

(a) 30.42 (b) 29.57

(c) 28.18 (d) 27.15

7. In an amplifier the load resistance R_L is equal to the plate resistance (r_p). The voltage amplification is equal to [DCE 2004]

[CPMT 1995]

(a) μ (b) 2μ

(c) $\mu/2$ (d) $\mu/4$

8. For a given plate-voltage, the plate current in a triode is maximum when the potential of

[IIT-JEE 1985; CPMT 1995; AFMC 1999]

(a) The grid is positive and plate is negative

(b) The grid is positive and plate is positive

(c) The grid is zero and plate is positive

(d) The grid is negative and plate is positive

9. If $R_p = 7K\Omega, g_m = 2.5$ *millimho*, then on increasing plate voltage by $50V$, how much the grid voltage is changed so that plate current remains the same [RPET 1996]
(a) – 2.86 V (b) – 4 V
(c) + 4 V (d) + 2 V

10. The amplification factor of a triode is 20 and trans-conductance is 3 *milli mho* and load resistance $3\times10^4\Omega$, then the voltage gain is
(a) 16.36 (b) 28
(c) 78 (d) 108

11. In a triode amplifier, $\mu = 25, r_p = 40$ kilo ohm and load resistance $R_L = 10$ kilo ohm. If the input signal voltage is 0.5 volt, then output signal voltage will be [RPMT 1995]
(a) 1.25 *volt* (b) 5 *volt*
(c) 2.5 *volt* (d) 10 *volt*

12. The amplification factor of a triode is 20. If the grid potential is reduced by 0.2 *volt* then to keep the plate current constant its plate voltage is to be increased by
[RPMT 1993, 95]
(a) 10 *volt* (b) 4 *volt*
(c) 40 *volt* (d) 100 *volt*

13. For a triode $r_p = 10$ *kilo ohm* and $g_m = 3$ *milli mho*. If the load resistance is double of plate resistance, then the value of voltage gain will be [RPMT 1994]
(a) 10 (b) 20
(c) 15 (d) 30

14. The amplification produced by a triode is due to the action of
(a) Filament (b) Cathode
(c) Grid (d) Plate

15. In an experiment, the saturation in the plate current in a diode is observed at 240 *V*. But a student still wants to increase the plate current. It can be done, if [MNR 1994]
(a) The plate voltage is increased further
(b) The plate voltage is decreased
(c) The filament current is decreased
(d) The filament current is increased

16. In a triode amplifier, the value of maximum gain is equal to
[MP PMT 1992]
(a) Half the amplification factor
(b) Amplification factor
(c) Twice the amplification factor
(d) Infinity

17. For a given triode $\mu = 20$. The load resistance is 1.5 times the anode resistance. The maximum gain will be
[CPMT 1992]
(a) 16 (b) 12
(c) 10 (d) None of the above

18. The voltage gain of a triode depends upon [CPMT 1992]
(a) Filament voltage (b) Plate voltage
(c) Plate resistance (d) Plate current

19. In a triode valve [MP PET 1992]
(a) If the grid voltage is zero then plate current will be zero
(b) If the temperature of filament is doubled, then the thermionic current will also be doubled
(c) If the temperature of filament is doubled, then the thermionic current will nearly be four times [RPMT 1996]
(d) At a definite grid voltage the plate current varies with plate voltage according to Ohm's law

20. The amplification factor of a triode valve is 15. If the grid voltage is changed by 0.3 *volt* the change in plate voltage in order to keep the plate current constant (in volt) is
[CPMT 1990]
(a) 0.02 (b) 0.002
(c) 4.5 (d) 5.0

21. The slope of plate characteristic of a vacuum tube diode for certain operating point on the curve is $10^{-3}\frac{mA}{V}$. The plate resistance of the diode and its nature respectively
[MP PMT 1990]
(a) 100 kilo-ohms static (b) 1000 *kilo-ohms* static
(c) 1000 *kilo-ohms* dynamic (d) 100 *kilo-ohms* dynamic

22. A triode has a mutual conductance of $2\times10^{-3}mho$ and an amplification factor of 50. The anode is connected through a resistance of 25×10^3 *ohms* to a 250 *volts* supply. The voltage gain of this amplifier is [MP PMT 1989]
(a) 50 (b) 25
(c) 100 [AFMC 1994] (d) 12.5

23. 14×10^{15} electrons reach the anode per second. If the power consumed is 448 *milliwatts*, then the plate (anode) voltage is
(a) 150 *V* (b) 200 *V*
(c) $14\times448V$ (d) 448/14 *V*

24. In the circuit of a triode valve, there is no change in the plate current, when the plate potential is increased from 200 *volt* to 220 *volt* and the grid potential is decreased from – 0.5 *volt* to –1.3 *volt*. The amplification factor of this valve is
[MP PMT 1989]
(a) 15 (b) 20
(c) 25 (d) 35

25. If the amplification factor of a triode (μ) is 22 and its plate resistance is 6600 *ohm*, then the mutual conductance of this valve is mho is [MP PMT 1989]
(a) $\frac{1}{300}$ (b) 25×10^{-2}
(c) 2.5×10^{-2} (d) 0.25×10^{-2}

26. For a triode, at $V_g = -1$ *volt*, the following observations were taken $V_p = 75V, I_p = 2mA$, $V_p = 100V, I_p = 4mA$. The value of plate resistance will be [MP PMT 1989]
(a) 25 $k\Omega$ (b) 20.8 $k\Omega$

(c) 12.5 $k\Omega$ (d) 100 $k\Omega$

27. The triode constant is out of the following [RPMT 1989]

(a) Plate resistance (b) Amplification factor

(c) Mutual conductance (d) All the above

28. The unit of mutual conductance of a triode valve is

[MP PMT 1988]

(a) Siemen (b) *Ohm*

(c) *Ohm metre* (d) *Joule Coulomb*

29. With a change of load resistance of a triode, used as an amplifier, from 50 *kilo ohms* to 100 *kilo ohms*, its voltage amplification changes from 25 to 30. Plate resistance of the triode is

(a) 25 $k\Omega$ (b) 75 $k\Omega$

(c) 7.5 $k\Omega$ (d) 2.5 $k\Omega$

30. Select the correct statements from the following

[IIT-JEE 1984]

(a) A diode can be used as a rectifier

(b) A triode cannot be used as a rectifier

(c) The current in a diode is always proportional to the applied voltage

(d) The linear portion of the I–V characteristic of a triode is used for amplification without distortion

31. The introduction of a grid in a triode valve affects plate current by

(a) Making the thermionic emission easier at low temperature

(b) Releasing more electrons from the plate

(c) By increasing plate voltage

(d) By neutralising space charge

32. Before the saturation state of a diode at the plate voltages of 400 V and 200 V respectively the currents are i_1 and i_2 respectively. The ratio i_1/i_2 will be

(a) $\sqrt{2}/4$ (b) $2\sqrt{2}$

(c) 2 (d) 1/2

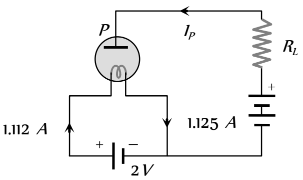
33. The value of plate current in the given circuit diagram will be

(a) 3 mA

(b) 8 mA

(c) 13 mA

(d) 18 mA



34. Coating of strontium oxide on Tungsten cathode in a valve is good for thermionic emission because [RPMT 1998]

(a) Work function decreases

(b) Work function increases

(c) Conductivity of cathode increases

(d) Cathode can be heated to high temperature

35. Correct relation for triode is [RPMT 2000]

(a) $\mu = g_m \times r_p$ (b) $\mu = \frac{g_m}{r_p}$

(c) $\mu = 2g_m \times r_p$ (d) None of these

36. Following is the relation between current and charge $I = AT^2 e^{qt/V_L}$ then value of V_L will be [RPMT 2000]

(a) $\frac{V}{kT}$ (b) $\frac{kV}{T}$

(c) $\frac{kT}{V}$ (d) $\frac{VT}{k}$

37. Which one is correct relation for thermionic emission

[RPMT 2000]

(a) $J = AT^{1/2} e^{-\phi/kT}$ (b) $J = AT^2 e^{-\phi/kT}$

(c) $J = AT^{3/2} e^{-\phi/kT}$ (d) $J = AT^2 e^{-\phi/2kT}$

[MP PET 1986]

38. When plate voltage in diode valve is increased from 100 *volt* to 150 *volt* then plate current increases from 7.5 *mA* to 12 *mA*. The dynamic plastic resistance will be [RPMT 2000]

(a) 10 $k\Omega$ (b) 11 $k\Omega$

(c) 15 $k\Omega$ (d) 11.1 $k\Omega$

39. In a diode valve, the state of saturation can be obtained easily by

(a) High plate voltage and high filament current

(b) Low filament current and high plate voltage

(c) Low plate voltage and high cathode temperature

(d) High filament current and high plate voltage

40. Plate resistance of two triode valves is 2 $k\Omega$ and 4 $k\Omega$, amplification factor of each of the valves is 40. The ratio of voltage amplification, when used with 4 $k\Omega$ load resistance, will be [CPMT 1975, 90]

(a) 10 (b) $\frac{4}{3}$

(c) $\frac{3}{4}$ (d) $\frac{16}{3}$

41. Diode is used as a/an [AIIMS 1999]

(a) Oscillator (b) Amplifier

(c) Rectifier (d) Modulator

42. The electrical circuits used to get smooth d.c. output from a rectifier circuit is called [KCET 2000]

(a) Filter (b) Amplifier

(c) Full wave rectifier (d) Oscillator

43. Which of the following does not vary with plate or grid voltages

(a) g_m (b) R_p

(c) μ (d) Each of them varies

44. The grid in a triode valve is used [UPSEAT 2000]

(a) To increases the thermionic emission

(b) To control the plate to cathode current

(c) To reduce the inter-electrode capacity

(d) To keep cathode at constant potential

45. In a triode valve the amplification factor is 20 and mutual conductance is 10^{-3} *mho*. The plate resistance is

[UPSEAT 2000]

(a) $2 \times 10^3\ \Omega$ (b) $4 \times 10^3\ \Omega$

(c) $2 \times 10^{4}\ \Omega$ (d) $2 \times 10^{4}\ \Omega$

46. The thermionic emission of electron is due to **[UPSEAT 2000]**

(a) Electromagnetic field (b) Electrostatic field

(c) High temperature (d) Photoelectric effect

47. The amplification factor of a triode is 50. If the grid potential is decreased by 0.20 *V*, what increase in plate potential will keep the plate current unchanged **[RPMT 1999]**

(a) 5 *V* (b) 10 *V*

(c) 0.2 *V* (d) 50 *V*

48. The slope of plate characteristic of a vacuum diode is $2 \times 10^{-2}\ mA/V$. The plate resistance of diode will be **[RPMT 1999]**

(a) 50 Ω (b) 50 *k*Ω

(c) 500 *k*Ω (d) 500 *k*Ω

49. The transconductance of a triode amplifier is 2.5 *mili mho* having plate resistance of 20 *k*Ω, amplification 10. Find the load resistance

(a) 5 *k*Ω (b) 25 *k*Ω

(c) 20 *k*Ω (d) 50 *k*Ω

50. The amplification factor of a triode is 18 and its plate resistance is 8 × 10Ω. A load resistance of 10Ω is connected in the plate circuit. The voltage gain will be **[RPMT 2002]**

(a) 30 (b) 20

(c) 10 (d) 1

51. The ripple factor in a half wave rectifier is **[RPMT 2002]**

(a) 1.21 (b) 0.48

(c) 0.6 (d) None of these

52. The correct relation for a triode is **[RPET 2000, 02]**

(a) $g_m = \left.\dfrac{\Delta I_p}{\Delta V_p}\right|_{V_g = constt.}$ (b) $g_m = \left.\dfrac{\Delta I_p}{\Delta V_g}\right|_{V_p = constt.}$

(c) Both (d) None of these

53. In a diode valve the cathode temperature must be (ϕ = work function) **[RPET 2002]**

(a) High and ϕ should be high

(b) High and ϕ should be low

(c) Low and ϕ should be high

(d) Low and ϕ should be high

54. The plate resistance of a triode is $2.5 \times 10^{4}\ \Omega$ and mutual conductance is 2×10^{-3} *mho*. What will be the value of amplification factor **[RPET 2002]**

(a) 50 (b) 1.25×10^{7}

(c) 75 (d) 2.25×10^{7}

55. Plate voltage of a triode is increased from 200 *V* to 225 *V*. To maintain the plate current, change in grid voltage from 5 *V* to 5.75 *V* is needed. The amplification factor is **[RPET 2002]**

(a) 40 (b) 45

(c) 33.3 (d) 25

56. The current in a triode at anode potential 100 *V* and grid potential – 1.2 *V* is 7.5 *mA*. If grid potential is changed to – 2.2 *V*, the current becomes 5.5 *mA*. the value of trans conductance (g) will be

(a) 2 *mili mho* (b) 3 *mili mho*

(c) 4 *mili mho* (d) 0.2 *mili mho*

57. Select the correct statement **[RPMT 2003]**

(a) In a full wave rectifier, two diodes work alternately

(b) In a full wave rectifier, two diodes work simultaneously

(c) The efficiency of full wave and half wave rectifiers is same

(d) The full wave rectifier is bi-directional

58. The amplification factor of a triode is 20. Its plate resistance is 10 kilo ohms. Mutual conductance is **[MNR 1992; Orissa JEE 2005]**

(a) 2×10^{5} *mho* (b) 2×10^{4} *mho*

(c) 500 *mho* (d) 2×10^{-3} *mho*

[RPMT 2001]

Critical Thinking

Objective Questions

1. A silicon speciman is made into a *P*-type semi-conductor by dopping, on an average, one Indium atom per 5×10^{7} silicon atoms. If the number density of atoms in the silicon specimen is 5×10^{28} atoms $/m^3$ then the number of acceptor atoms in silicon per cubic centimetre will be [MP PMT 1993, 2003]

(a) $2.5\times10^{30}\,atoms/cm^3$ (b) $1.0\times10^{13}\,atoms/cm^3$

(c) $1.0\times10^{15}\,atoms/cm^3$ (d) $2.5\times10^{36}\,atoms/cm^3$

2. The probability of electrons to be found in the conduction band of an intrinsic semiconductor at a finite temperature [IIT-JEE 1995; DPMT 2004]

(a) Decreases exponentially with increasing band gap

(b) Increases exponentially with increasing band gap

(c) Decreases with increasing temperature

(d) Is independent of the temperature and the band gap

3. The typical ionisation energy of a donor in silicon is [IIT-JEE 1992]

(a) $10.0\,eV$ (b) $1.0\,eV$

(c) $0.1\,eV$ (d) $0.001\,eV$

4. In *PN*-junction diode the reverse saturation current is 10^{-5} *amp* at $27°C$. The forward current for a voltage of $0.2 volt$ is

(a) $2037.6\times10^{-3}amp$ (b) $203.76\times10^{-3}amp$

(c) $20.376\times10^{-3}amp$ (d) $2.0376\times10^{3}amp$

$[\exp(7.62)=2038.6, K=1.4\times10^{-23}\,J/K]$

5. When a potential difference is applied across, the current passing through [IIT-JEE 1999]

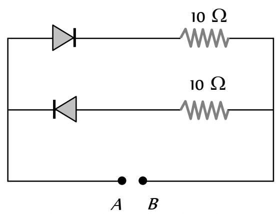
(a) An insulator at $0K$ is zero

(b) A semiconductor at $0K$ is zero

(c) A metal at $0K$ is finite

(d) A *P-N* diode at $300K$ is finite, if it is reverse biased

6. A 2 *V* battery is connected across the points *A* and *B* as shown in the figure given below. Assuming that the resistance of each diode is zero in forward bias and infinity in reverse bias, the current supplied by the battery when its positive terminal is connected to *A* is [UPSEAT 2002]



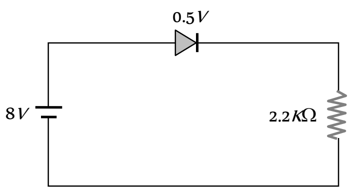
(a) 0.2 *A*

(b) 0.4 *A*

(c) Zero

(d) 0.1 *A*

7. In the circuit, if the forward voltage drop for the diode is 0.5 *V*, the current will be [UPSEAT 2003]



(a) 3.4 *mA*

(b) 2 *mA*

(c) 2.5 *mA*

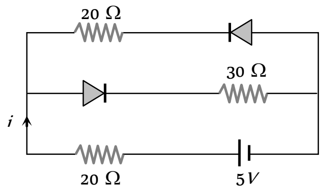
(d) 3 *mA*

8. A *P*-type semiconductor has acceptor levels 57 *meV* above the valence band. The maximum wavelength of light required to create a hole is (Planck's constant $h = 6.6\times10^{-34}$ *J-s*)

(a) 57 $Å$ (b) 57×10^{-3} $Å$

(c) 217100 $Å$ (d) 11.61×10^{-33} $Å$

9. Current in the circuit will be [CBSE PMT 2001]



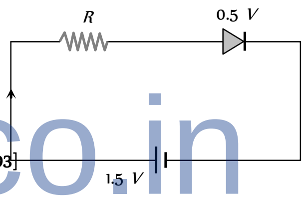
(a) $\frac{5}{40}A$

(b) $\frac{5}{50}A$

(c) $\frac{5}{10}A$

(d) $\frac{5}{20}A$

10. The diode used in the circuit shown in the figure has a constant voltage drop of 0.5 *V* at all currents and a maximum power rating of 100 *milliwatts*. What should be the value of the resistor *R*, connected in series with the diode for obtaining maximum current [CBSE PMT



[MP PMT 1993]

(a) 1.5 Ω

(b) 5 Ω

(c) 6.67 Ω

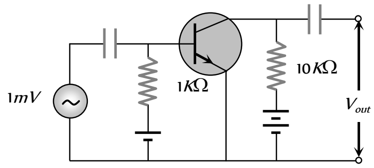
(d) 200 Ω

11. For a transistor amplifier in common emitter configuration for load impedance of 1 *k*Ω (h_{fe} = 50 and h_{oe} = 25 $\mu A/V$) the current gain is

(a) – 5.2 (b) – 15.7

(c) – 24.8 (d) – 48.78

12. In the following common emitter configuration an *NPN* transistor with current gain β = 100 is used. The output voltage of the amplifier will be [AIIMS 2003]



(a) 10 *mV*

(b) 0.1 *V*

(c) 1.0 *V*

(d) 10 *V*

13. In semiconductor the concentrations of electrons and holes are $8\times10^{18}/m^3$ and $5\times10^{18}/m^3$ respectively. If the mobilities of electrons and hole are 2.3 $m^2/volt\text{-}sec$ and 0.01 $m^2/volt\text{-}sec$ respectively, then semiconductor is

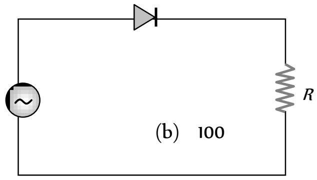
(a) *N*-type and its resistivity is 0.34 *ohm-metre*

(b) *P*-type and its resistivity is 0.034 *ohm-metre*

(c) *N*-type and its resistivity is 0.034 *ohm-metre*

(d) *P*-type and its resistivity is 3.40 *ohm-metre*

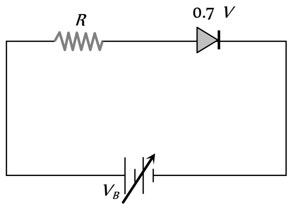
14. A sinusoidal voltage of peak value 200 *volt* is connected to a diode and resistor R in the circuit shown so that half wave rectification occurs. If the forward resistance of the diode is negligible compared to R the *rms* voltage (in *volt*) across R is approximately



(a) 200 (b) 100

(c) $\frac{200}{\sqrt{2}}$ (d) 280

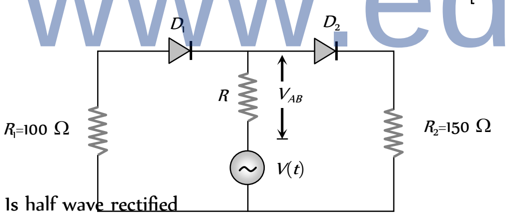
15. The junction diode in the following circuit requires a minimum current of 1 mA to be above the knee point (0.7 V) of its I-V characteristic curve. The voltage across the diode is independent of current above the knee point. If V_B = 5 V, then the maximum value of R so that the voltage is above the knee point, will be



(a) 4.3 $k\Omega$ (b) 860 $k\Omega$

(c) 4.3 Ω (d) 860 Ω

16. In the circuit given below, $V(t)$ is the sinusoidal voltage source, voltage drop $V_{AB}(t)$ across the resistance R is [IIT 1993]



(a) Is half wave rectified

(b) Is full wave rectified

(c) Has the same peak value in the positive and negative half cycles

(d) Has different peak values during positive and negative half cycle

17. The peak voltage in the output of a half-wave diode rectifier fed with a sinusoidal signal without filter is 10 V. The dc component of the output voltage is [CBSE PMT 2004]

(a) $10/\sqrt{2}\ V$ (b) $10/\pi\ V$

(c) 10 V (d) $20/\pi\ V$

18. A transistor is used as an amplifier in CB mode with a load resistance of 5 $k\,\Omega$ the current gain of amplifier is 0.98 and the input resistance is 70 Ω, the voltage gain and power gain respectively are [Pb. PET 2003]

(a) 70, 68.6 (b) 80, 75.6

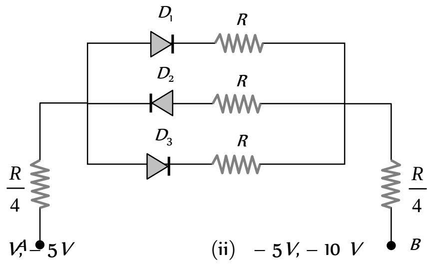
(c) 60, 66.6 (d) 90, 96.6

19. The Bohr radius of the fifth electron of phosphorus (atomic number = 15) acting as dopant in silicon (relative dielectric constant = 12) is

(a) 10.6 Å (b) 0.53 Å

(c) 21.2 Å (d) None of these

20. In the following circuits PN-junction diodes D_1, D_2 and D_3 are ideal for the following potential of A and B, the correct increasing order of resistance between A and B will be



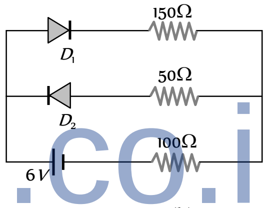
(i) – 10 V, – 5 V (ii) – 5 V, – 10 V

(iii) – 4 V, – 12 V

(a) (i) < (ii) < (iii) (b) (iii) < (ii) < (i)

(c) (ii) = (iii) < (i) (d) (i) = (iii) < (ii)

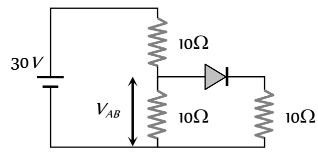
21. The circuit shown in following figure contains two diode D_1 and D_2 each with a forward resistance of 50 *ohms* and with infinite backward resistance. If the battery voltage is 6 V, the current through the 100 *ohm* resistance (in *amperes*) is [IIT-JEE 1997]



(a) Zero (b) 0.02

(c) 0.03 (d) 0.036

22. Find V_{AB} [RPMT 2000]



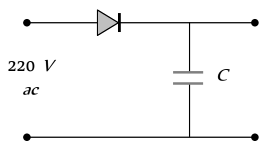
(a) 10 V

(b) 20 V

(c) 30 V

(d) None of these

23. A diode is connected to 220 V (*rms*) *ac* in series with a capacitor as shown in figure. The voltage across the capacitor is



(a) 220 V

(b) 110 V

(c) 311.1 V

(d) $\frac{220}{\sqrt{2}}\ V$

24. A potential difference of 2 V is applied between the opposite faces of a Ge crystal plate of area 1 cm^2 and thickness 0.5 mm. If the concentration of electrons in Ge is $2 \times 10^{19}/m^3$ and mobilities of electrons and holes are $0.36\frac{m^2}{volt-\sec}$ and $0.14\frac{m^2}{volt-\sec}$ respectively, then the current flowing through the plate will be

(a) 0.25 *A* (b) 0.45 *A*

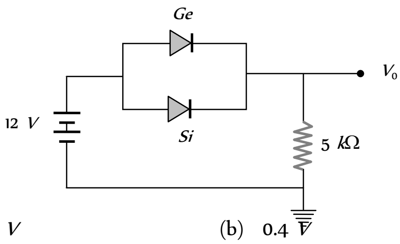
(c) 0.56 *A* (d) 0.64 *A*

25. The contribution in the total current flowing through a semiconductor due to electrons and holes are $\frac{3}{4}$ and $\frac{1}{4}$ respectively. If the drift velocity of electrons is $\frac{5}{2}$ times that of holes at this temperature, then the ratio of concentration of electrons and holes is

(a) 6 : 5 (b) 5 : 6

(c) 3 : 2 (d) 2 : 3

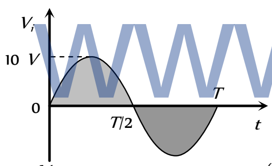
26. *Ge* and *Si* diodes conduct at 0.3 *V* and 0.7 *V* respectively. In the following figure if *Ge* diode connection are reversed, the valve of V_o changes by [Based on Roorkee 2000]

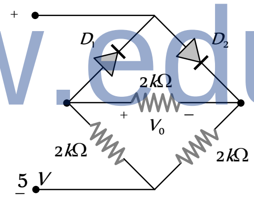


(a) 0.2 *V* (b) 0.4 *V*

(c) 0.6 *V* (d) 0.8 *V*

27. In the circuit shown in figure the maximum output voltage V_o is





(a) 0 *V* (b) 5 *V*

(c) 10 *V* (d) $\frac{5}{\sqrt{2}}V$

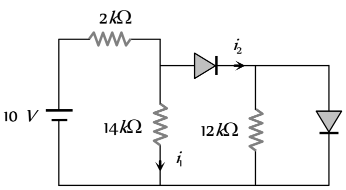
28. In the following circuit find I_1 and I_2

(a) 0, 0

(b) 5 *mA*, 5 *mA*

(c) 5 *mA*, 0

(d) 0, 5 *mA*



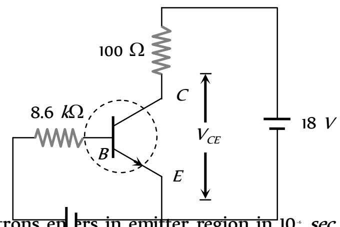
29. For the transistor circuit shown below, if β = 100, voltage drop between emitter and base is 0.7 *V* then value of V_{CE} will be

(a) 10 *V*

(b) 5 *V*

(c) 13 *V*

(d) 0 *V*



30. In *NPN* transistor, 10^{10} electrons enters in emitter region in 10^{-6} *sec*. If 2% electrons are lost in base region then collector current and current amplification factor (β) respectively are

(a) 1.57 *mA*, 49 (b) 1.92 *mA*, 70

(c) 2 *mA*, 25 (d) 2.25 *mA*, 100

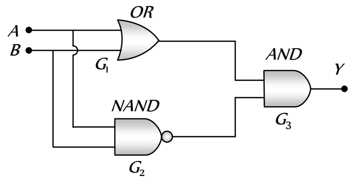
31. The following configuration of gate is equivalent to [AMU 1999]

(a) NAND

(b) XOR

(c) OR

(d) None of these



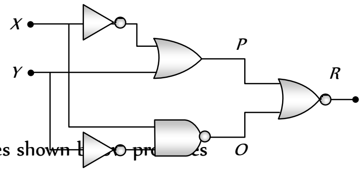
32. Figure gives a system of logic gates. From the study of truth table it can be found that to produce a high output (1) at *R*, we must have

(a) *X* = 0, *Y* = 1

(b) *X* = 1, *Y* = 1

(c) *X* = 1, *Y* = 0

(d) *X* = 0, *Y* = 0



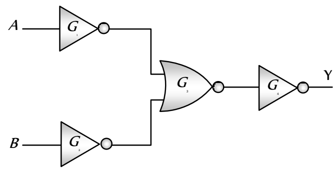
33. The combination of gates shown below produces

(a) AND gate

(b) XOR gate

(c) NOR gate

(d) NAND gate



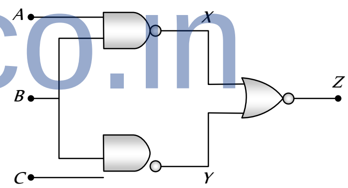
34. The shows two NAND gates followed by a NOR gate. The system is equivalent to the following logic gate

(a) OR

(b) AND

(c) NAND

(d) None of these



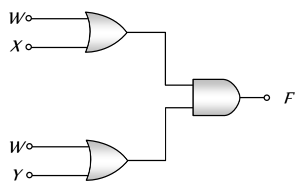
35. The diagram of a logic circuit is given below. The output *F* of the circuit is represented by

(a) $W.(X+Y)$

(b) $W\cdot(X\cdot Y)$

(c) $W+(X\cdot Y)$

(d) $W+(X+Y)$



36. The plate current i_p in a triode valve is given $i_p = K(V_p + \mu V_g)^{3/2}$ where i_p is in milliampere and V_p and V_g are in *volt*. If r_p = 10^4 *ohm*, and $g_m = 5\times10^{-3} mho$, then for $i_p = 8\,mA$ and $V_p = 300\,volt$, what is the value of *K* and grid cut off voltage [Roorkee 1992]

(a) – 6 *V*, $(30)^{3/2}$ (b) $-6V,(1/30)^{3/2}$

(c) + 6 *V*, $(30)^{3/2}$ (d) + 6 *V*, $(1/30)^{3/2}$

37. The linear portions of the characteristic curves of a triode valve give the following readings [Roorkee 1985]

V_g (*volt*)	0	– 2	– 4	– 6

$I_p(mA)$ for $V_p = 150$ *volts*	15	12.5	10	7.5
$I_p(mA)$ for $V_p = 120$ *volts*	10	7.5	5	2.5

The plate resistance is

(a) 2000 *ohms* (b) 4000 *ohms*

(c) 8000 *ohms* (d) 6000 *ohms*

38. The relation between dynamic plate resistance (r) of a vacuum diode and plate current in the space charge limited region, is

(a) $r_p \propto I_p$ (b) $r_p \propto I_p^{3/2}$

(c) $r_p \propto \frac{1}{I_p}$ (d) $r_p \propto \frac{1}{(I_p)^{1/3}}$

39. The relation between I_p and V_p for a triode is

$$I_p = (0.125V_p - 7.5)mA$$

Keeping the grid potential constant at 1*V*, the value of r_p will be

(a) 8 $k\Omega$ (b) 4 $k\Omega$

(c) 2 $k\Omega$ (d) 8 $k\Omega$

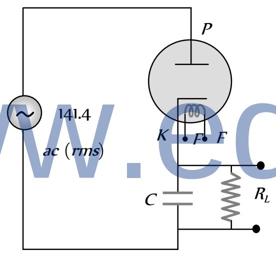
40. An alternating voltage of 141.4 *V* (*rms*) is applied to a vacuum diode as shown in the figure. The maximum potential difference across the condenser will be

(a) 100 *V*

(b) 200 *V*

(c) $100\sqrt{2}V$

(d) $200\sqrt{2}V$



41. A metallic surface with work function of 2 *eV*, on heating to a temperature of 800 *K* gives an emission current of 1 *mA*. If another metallic surface having the same surface area, same emission constant but work function 4 *eV* is heated to a temperature of 1600 *K*, then the emission current will be

(a) 1 *mA* (b) 2 *mA*

(c) 4 *mA* (d) None of these

42. A change of 0.8 *mA* in the anode current of a triode occurs when the anode potential is changed by 10 *V*. If μ = 8 for the triode, then what change in the grid voltage would be required to produce a change of 4 *mA* in the anode current

(a) 6.25 *V* (b) 0.16 *V*

(c) 15.2 *V* (d) None of these

43. The plate current in a triode is given by

$$I_p = 0.004\,(V_p + 10V_g)^{3/2} mA$$

where I_p, V_p and V_g are the values of plate current, plate voltage and grid voltage, respectively. What are the triode parameters μ, r_p and g_m for the operating point at $V_p = 120\,volt$ and $V_g = -2\,volt$?

(a) 10, 16.7 $k\Omega$, 0.6 *m mho* (b) 15, 16.7 $k\Omega$, 0.06 *m mho*

(c) 20, 6 $k\Omega$, 16.7 *m mho* (d) None of these

44. A triode whose mutual conductance is 2.5 *m A/volt* and anode resistance is 20 *kilo ohm*, is used as an amplifier whose amplification is 10. The resistance connected in plate circuit will be [MP PET 1989; RPMT 1998]

(a) 1 $k\Omega$ (b) 5 $k\Omega$

(c) 10 $k\Omega$ (d) 20 $k\Omega$

45. In the grid circuit of a triode a signal $E = 2\sqrt{2}\cos\omega t$ is applied. If μ = 14 and r_p =10 $k\Omega$ then root mean square current flowing through $R_L = 12\,k\Omega$ will be

(a) 1.27 *mA* (b) 10 *mA*

(c) 1.5 *mA* (d) 12.4 *mA*

46. For a triode μ = 64 and g_m =1600 μ *mho*. It is used as an amplifier and an input signal of 1 *V* (*rms*) is applied. The signal power in the load of 40 $k\Omega$ will be

(a) 23.5 *mW* (b) 48.7 *mW*

(c) 25.6 *mW* (d) None of these

47. Amplification factor of a triode is 10. When the plate potential is 200 *volt* and grid potential is – 4 *volt*, then the plate current of 4 *mA* is observed. If plate potential is changed to 160 *volt* and grid potential is kept at – 7 *volt*, then the plate current will be

(a) 1.69 *mA* (b) 3.95 *mA*

(c) 2.87 (d) 7.02 *mA*

48. On applying a potential of – 1 *volt* at the grid of a triode, the following relation between plate voltage V_p (*volt*) and plate current $I_p(\text{in}\,mA)$ is found

$$I_p = 0.125\,V_p - 7.5$$

If on applying – 3 *volt* potential at grid and 300 *V* potential at plate, the plate current is found to be 5 *mA*, then amplification factor of the triode is

(a) 100 (b) 50

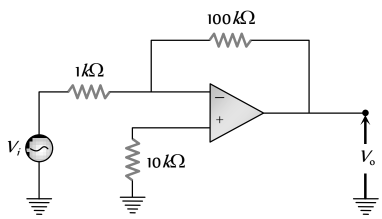
(c) 30 (d) 20

49. The slopes of anode and mutual characteristics of a triode are 0.02 *mA V* and 1 *mA V* respectively. What is the amplification factor of the valve [MP PMT 1990]

(a) 5 (b) 50

(c) 500 (d) 0.5

50. The voltage gain of the following amplifier is [AIIMS 2005]

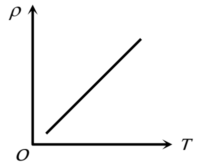


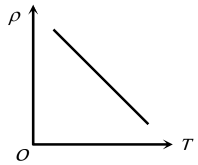
(a) 10 (b) 100

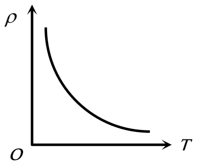
(c) 1000 (d) 9.9

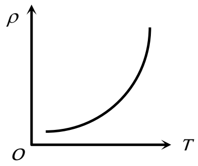
Graphical Questions

1. The temperature (T) dependence of resistivity (ρ) of a semiconductor is represented by [AIIMS 2004]

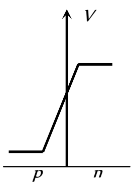
(a)


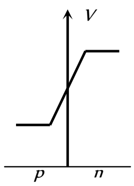
(b)


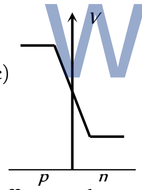
(c)


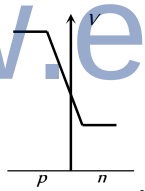
(d)


2. In a forward biased PN-junction diode, the potential barrier in the depletion region is of the form ... [KCET 2004]

(a)


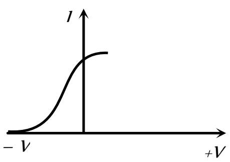
(b)


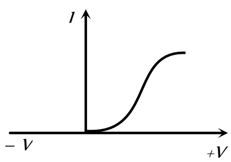
(c)


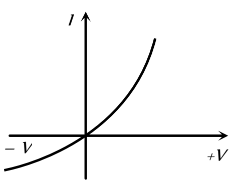
(d)


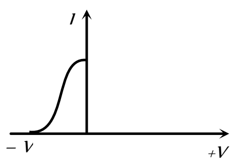
3. Different voltages are applied across a P-N junction and the currents are measured for each value. Which of the following graphs is obtained between voltage and current

[MP PET 1996; UPSEAT 2002]

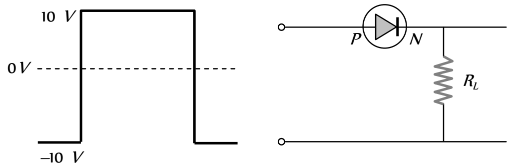
(a)


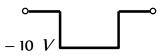
(b)


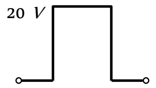
(c)


(d)


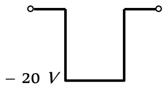
4. If the following input signal is sent through a *PN*-junction diode, then the output signal across R_L will be



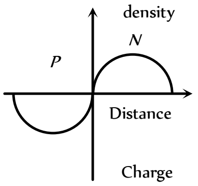
(a) 

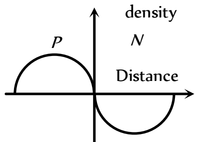
(b) 

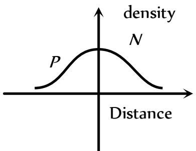
(c) 

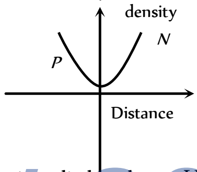
(d) 

5. The curve between charge density and distance near *P-N* junction will be

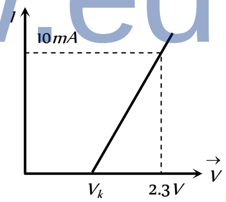
(a) 

(b) 

(c) 

(d) 

6. The resistance of a germanium junction diode whose $V-I$ is shown in figure is ($V_k = 0.3V$)



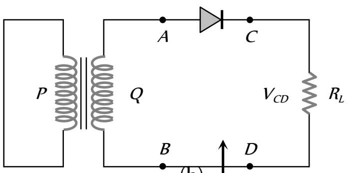
(a) 5 $k\Omega$

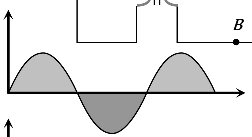
(b) 0.2 $k\Omega$

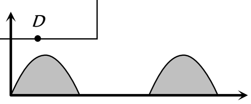
(c) 2.3 $k\Omega$

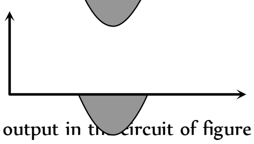
(d) $\left(\frac{10}{2.3}\right)k\Omega$

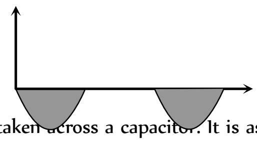
7. In the half-wave rectifier circuit shown. Which one of the following wave forms is true for V_{CD}, the output across *C* and *D*?



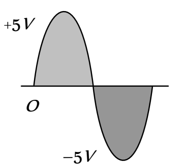
(a) 

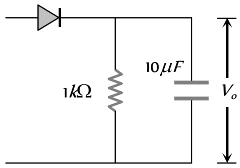
(b) 

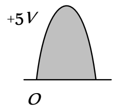
(c) 

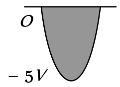
(d) 

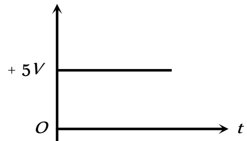
8. The output in the circuit of figure is taken across a capacitor. It is as shown in figure

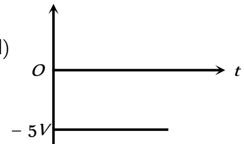




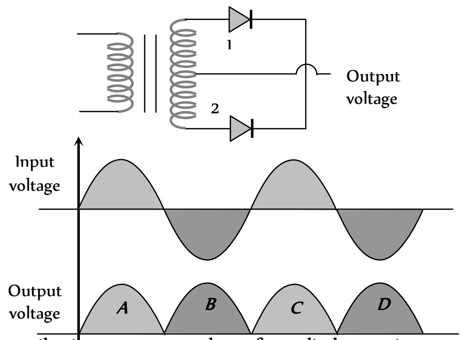
(a) 

(b) 

(c) 

(d) 

9. A full wave rectifier circuit along with the input and output voltages is shown in the figure



The contribution to output voltage from diode – 2 is

[MP PMT 2001]

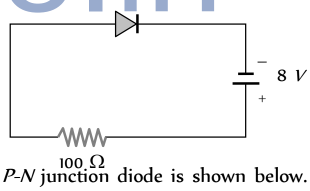
(a) *A*, *C*

(b) *B*, *D*

(c) *B*, *C*

(d) *A*, *D*

10. A source voltage of 8 *V* drives the diode in fig. through a current-limiting resistor of 100 *ohm*. Then the magnitude of the slope load line on the *V-I* characteristics of the diode is



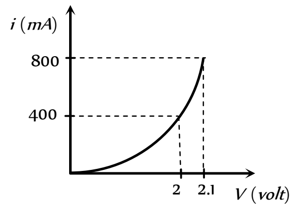
(a) 0.01

(b) 100

(c) 0.08

(d) 12.5

11. The *i-V* characteristic of a *P-N* junction diode is shown below. The approximate dynamic resistance of the *P-N* junction when a forward bias of 2 *volt* is applied



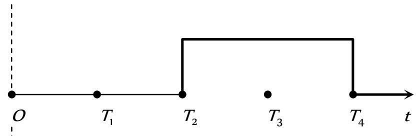
(a) 1 Ω

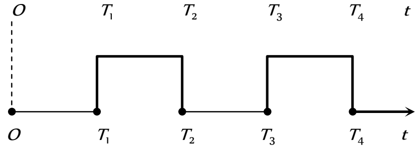
(b) 0.25 Ω

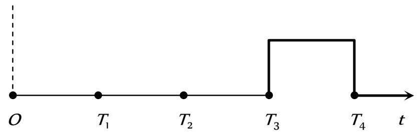
(c) 0.5 Ω

(d) 5 Ω

12. The given figure shows the wave forms for two inputs *A* and *B* and that for the output *Y* of a logic circuit. The logic circuit is

(A) 

(B) 

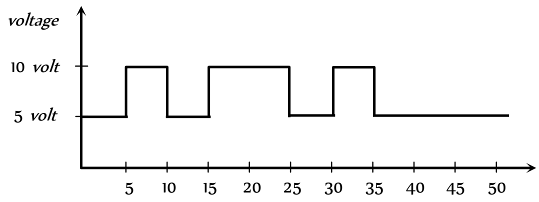


(Y)

(a) An AND gate (b) An OR gate

(c) A NAND gate (d) An NOT gate

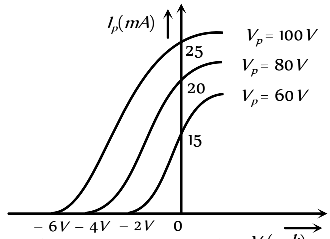
13. In a negative logic the following wave form corresponds to the



(a) 0000000000 (b) 000

(c) 111111111 (d) 1010010111

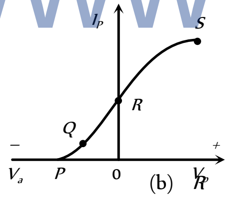
14. The variation of anode current in a triode corresponding to a change in grid potential at three different values of the plate potential is shown in the diagram. The mutual conductance of the triode is



(a) 2.5 $m\ mho$ (b) 5.0 $m\ mho$

(c) 7.5 $m\ mho$ (d) 10.0 $m\ mho$

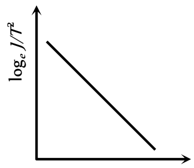
15. The point representing the cut off grid voltage on the mutual characteristic of triode is

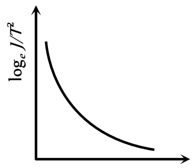


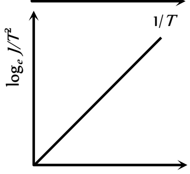
(a) S (b) R

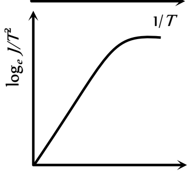
(c) O (d) P

16. For a thermionic emitter (metallic) if J represents the current density and T is its absolute temperature then the correct curve between $\log_e \frac{J}{T^2}$ and $\frac{1}{T}$ is

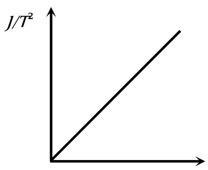
(a) 

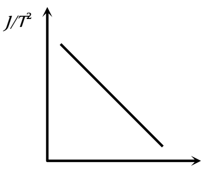
(b) 

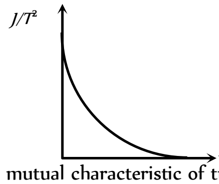
(c) 

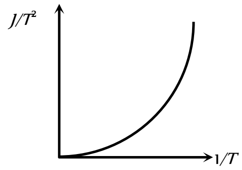
(d) 

17. If the thermionic current density is J and emitter temperature is T then the curve between $\frac{J}{T^2}$ and $\frac{1}{T}$ will be

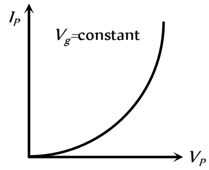
(a) 

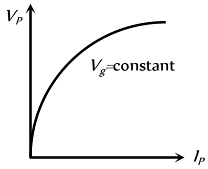
(b) 

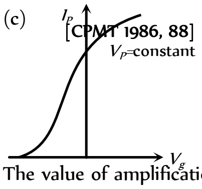
(c) 

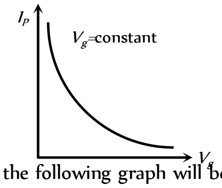
(d) 

18. The mutual characteristic of triode is

(a) 

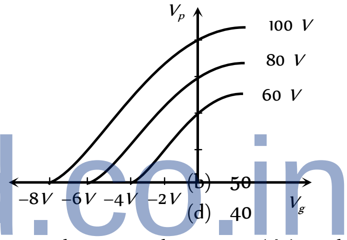
(b) 

(c) 

(d) 

[CPMT 1986, 88]

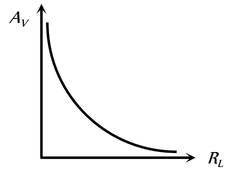
19. The value of amplification factor from the following graph will be

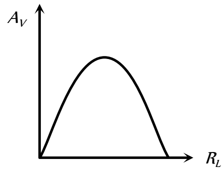


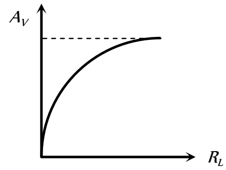
(a) 10 (b) 50

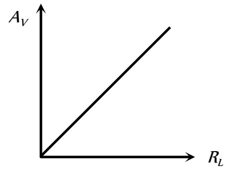
(c) 25 (d) 40

20. The correct curve between voltage gain (A_v) and load resistance (R_L) is

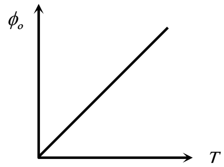
(a) 

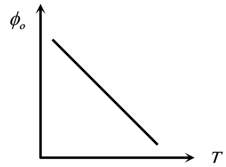
(b) 

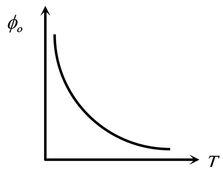
(c) 

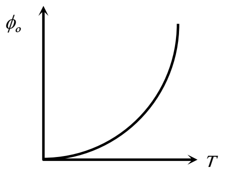
(d) 

21. The curve between the work function of a metal (ϕ_o) and its temperature (T) will be

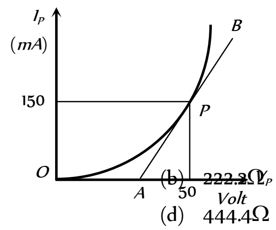
(a) 

(b) 

(c) 

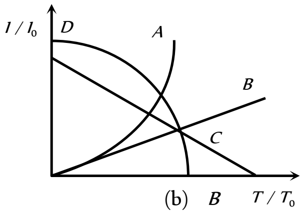
(d) 

22. The plate characteristic curve of a diode in space charge limited region is as shown in the figure. The slope of curve at point P is 5.0 mA/V. The static plate resistance of diode will be



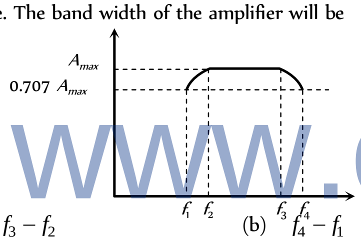
(a) 111.1Ω (b) 222.2Ω
(c) 333.3Ω (d) 444.4Ω

23. The ratio of thermionic currents (I/I_0) for a metal when the temperature is slowly increased T_0 to T as shown in figure. (I and I_0 are currents at T and respectively). Then which one is correct?



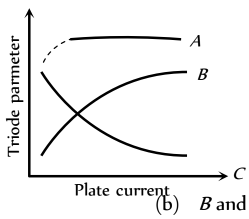
(a) A (b) B
(c) C (d) D

24. The frequency response curve of RC coupled amplifier is shown in figure. The band width of the amplifier will be



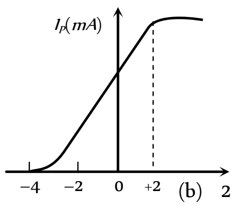
(a) $f_3 - f_2$ (b) $f_4 - f_1$
(c) $\frac{f_4 - f_2}{2}$ (d) $f_3 - f_1$

25. The figure represents variation of triode parameter (μ or r_p or g_m) with the plate current. The correct variation of μ and r_p are given, respectively by the curves



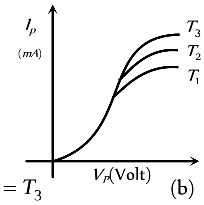
(a) A and B (b) B and C
(c) A and C (d) None of the above

26. The mutual characteristic curves of a triode are as shown in figure. The cut off voltage for the triode is



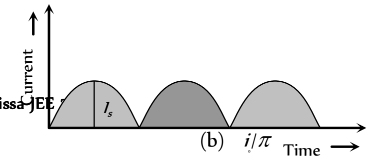
(a) 0 V (b) 2 V
(c) – 4 V (d) 6 V

27. For the diode, the characteristic curves are given at different temperature. The relation between the temperatures is [RPET 1990]



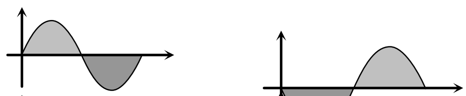
(a) $T_1 = T_2 = T_3$ (b) $T_1 < T_2 < T_3$
(c) $T_1 > T_2 > T_3$ (d) None of the above

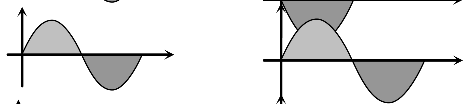
28. The output current versus time curve of a rectifier is shown in the figure. The average value of the output current in this case is [Orissa JEE]

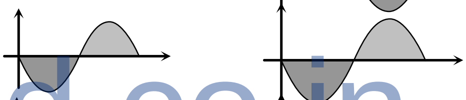


(a) 0 (b) i_0/π
(c) $2i_0/\pi$ (d) i_0

29. Which of the following figures correctly shows the phase relation between the input signal and the output signal of triode amplifier

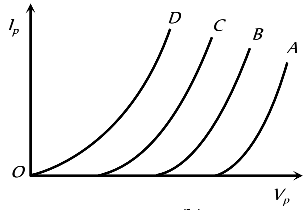
(a)


(b)


(c)


(d)


30. In the figure four plate characteristics of a triode at different grid voltage are shown. The difference between successive grid voltage is 1 V. Which curve will have maximum grid voltage and what is its value?



(a) A, V_g = + 4 V (b) B, V_g = + 4 V
(c) A, V_g = 0 (d) D, V_g = 0

AR Assertion & Reason

For AIIMS Aspirants

Read the assertion and reason carefully to mark the correct option out of the options given below:

(a) *If both assertion and reason are true and the reason is the correct explanation of the assertion.*
(b) *If both assertion and reason are true but reason is not the correct explanation of the assertion.*
(c) *If assertion is true but reason is false.*
(d) *If the assertion and reason both are false.*
(e) *If assertion is false but reason is true.*

1. Assertion : The logic gate NOT can be built using diode.

Reason : The output voltage and the input voltage of the diode have 180° phase difference.

[AIIMS 2005]

2. Assertion : The number of electrons in a *P*-type silicon semiconductor is less than the number of electrons in a pure silicon semiconductor at room temperature.

Reason : It is due to law of mass action. [AIIMS 2005]

3. Assertion : In a common emitter transistor amplifier the input current is much less than the output current.

Reason : The common emitter transistor amplifier has very high input impedance. [AIIMS 2005]

4. Assertion : A transistor amplifier in common emitter configuration has a low input impedence.

Reason : The base to emitter region is forward biased.

[AIIMS 2004]

5. Assertion : The resistivity of a semiconductor increases with temperature.

Reason : The atoms of a semiconductor vibrate with larger amplitude at higher temperature there by increasing it's resistivity. [AIIMS 2003]

6. Assertion : If the temperature of a semiconductor is increased then it's resistance decreases.

Reason : The energy gap between conduction band and valence band is very small [AIIMS 1997]

7. Assertion : The temperature coefficient of resistance is positive for metals and negative for *P-type* semiconductor.

Reason : The effective charge carriers in metals are negatively charged whereas in *P*-type semiconductor they are positively charged.

[AIIMS 1996]

8. Assertion : Electron has higher mobility than hole in a semiconductor.

Reason : Mass of electron is less than the mass of hole.

9. Assertion : An *N*-type semiconductor has a large number of electrons but still it is electrically neutral.

Reason : An *N*-type semiconductor is obtained by doping an intrinsic semiconductor with a pentavalent impurity.

10. Assertion : The crystalline solids have a sharp melting point.

Reason : All the bonds between the atoms or molecules of a crystalline solids are equally strong, that they get broken at the same temperature.

11. Assertion : Silicon is preferred over germanium for making semiconductor devices.

Reason : The energy gap for germanium is more than the energy gap of silicon.

12. Assertion : We can measure the potential barrier of a *PN* junction by putting a sensitive voltmeter across its terminals.

Reason : The current through the *PN* junction is not same in forward and reversed bias.

13. Assertion : Semiconductors do not Obey's Ohm's law.

Reason : Current is determined by the rate of flow of charge carriers.

14. Assertion : Two P-N junction diodes placed back to back, will work as a NPN transistor.

Reason : The P-region of two PN junction diodes back to back will form the base of NPN transistor.

15. Assertion : In transistor common emitter mode as an amplifier is preferred over common base mode.

Reason : In common emitter mode the input signal is connected in series with the voltage applied to the base emitter function.

16. Assertion : The dominant mechanism for motion of charge carriers in forward and reverse biased silicon P-N junction are drift in both forward and reverse bias.

Reason : In reverse biasing, no current flow through the junction.

17. Assertion : A transistor is a voltage-operating device.

Reason : Base current is greater than the collector current.

18. Assertion : NAND or NOR gates are called digital building blocks.

Reason : The repeated use of NAND (or NOR) gates can produce all the basic or complicated gates.

19. Assertion : At 0 K Germanium is a superconductor.

Reason : At 0 K Germanium offers zero resistance.

20. Assertion : Base in a transistor is made very thin as compared to collector and emitter regions.

Reason : Due to thin base power gain and voltage gain is obtained by a transistor.

21. Assertion : The current gain in common base circuit is always less than one.

Reason : At constant collector voltage the change in collector current is more than the change in emitter current.

22. Assertion : V-i characteristic of P-N junction diode is same as that of any other conductor.

Reason : P-N junction diode behave as conductor at room temperature.

23. Assertion : Zener diode works on a principle of breakdown voltage.

Reason : Current increases suddenly after breakdown voltage.

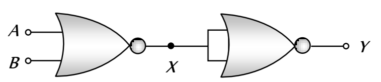
24. Assertion : NOT gate is also called inverter circuit.

Reason : NOT gate inverts the input order.

25. Assertion : In vacuum tubes (valves), vacuum is necessary for the movement of electrons between electrodes otherwise electrons collide with air particle and loses their energy.

Reason : In semiconductors devices, external heating or vacuum is not required.

26. Assertion : The following circuit represents 'OR' gate



Reason : For the above circuit $Y = \overline{X} = \overline{\overline{A+B}} = A+B$

27. Assertion : A P-N photodiode is made from a semiconductor for which E_g = 2.8 eV. This photo diode will not detect the wavelength of 6000 nm.

Reason : A PN photodiode detect wavelength λ if $\frac{hc}{\lambda} > E_g$.

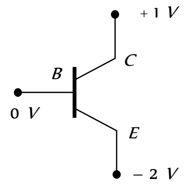
28. Assertion : 29 is the equivalent decimal number of binary number 11101.

Reason : $(11101)_2 = (1\times2^4 + 1\times2^3 + 1\times2^2 + 0\times2^1 + 1\times2^0)_{10}$

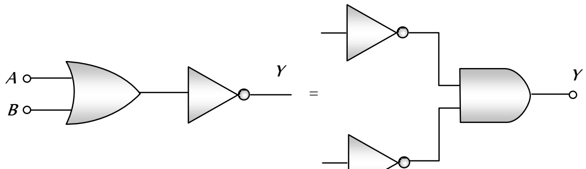
$= (16 + 8 + 4 + 0 + 1)_{10} = (29)_{10}$

29. Assertion : When PN-junction is forward biased then motion of charge carriers at junction is due to diffusion. In reverse biasing. The cause of motion of charge is drifting.

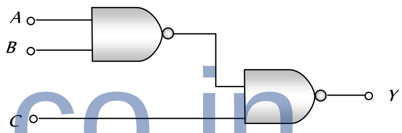
Reason : In the following circuit emitter is reverse biased and collector is forward biased.



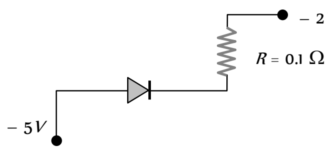
30. Assertion : De-morgan's theorem $\overline{A+B} = \overline{A}\cdot\overline{B}$ may be explained by the following circuit



Reason : In the following circuit, for output inputs ABC are 101



31. Assertion : In the following circuit the potential drop across the resistance is zero.



Reason : The given resistance has low value.

Answers

Solids and Crystals

1	d	2	d	3	d	4	a	5	a
6	a	7	a	8	b	9	a	10	c
11	d	12	c	13	b	14	a	15	a
16	a	17	d	18	b	19	c	20	c
21	b	22	a	23	b	24	a	25	d
26	d	27	d	28	d				

Semiconductors

1	c	2	b	3	d	4	b	5	b
6	b	7	b	8	c	9	d	10	a
11	b	12	a	13	a	14	d	15	c
16	b	17	b	18	b	19	c	20	c
21	d	22	b	23	ac	24	d	25	b
26	c	27	d	28	c	29	c	30	b
31	d	32	a	33	b	34	a	35	c
36	d	37	c	38	b	39	d	40	a
41	d	42	c	43	b	44	c	45	d
46	b	47	a	48	b	49	a	50	d
51	d	52	b	53	b	54	a	55	c
56	d	57	b	58	d	59	a	60	a
61	b	62	a	63	c	64	a	65	b
66	a	67	c	68	c	69	c	70	c
71	b	72	b	73	a	74	b	75	c
76	b	77	c	78	a	79	d	80	a
81	a	82	a	83	b	84	d	85	c
86	d	87	a	88	c	89	b	90	c
91	a	92	b	93	d	94	d	95	d
96	d	97	d	98	a	99	b	100	a
101	b								

Semiconductor Diode

1	b	2	a	3	b	4	b	5	c
6	b	7	a	8	b	9	a	10	a
11	b	12	b	13	b	14	c	15	d
16	c	17	c	18	bc	19	c	20	d
21	d	22	b	23	d	24	c	25	c
26	b	27	b	28	b	29	c	30	b
31	b	32	c	33	d	34	c	35	d
36	a	37	b	38	b	39	d	40	a
41	b	42	a	43	b	44	a	45	a
46	b	47	b	48	a	49	c	50	d
51	d	52	a	53	c	54	c	55	b
56	d	57	a	58	a	59	c	60	a
61	b	62	c	63	a	64	c	65	a
66	b	67	c	68	c	69	d	70	a
71	c	72	a	73	d	74	d	75	c
76	a	77	c	78	c	79	c		

Junction Transistor

1	a	2	c	3	a	4	d	5	d
6	b	7	d	8	b	9	b	10	b
11	c	12	d	13	d	14	a	15	b
16	b	17	d	18	b	19	ac	20	a
21	c	22	a	23	b	24	b	25	b
26	c	27	a	28	b	29	b	30	d
31	b	32	b	33	a	34	b	35	b
36	a	37	a	38	a	39	b	40	a
41	b	42	d	43	d	44	b		

Digital Electronics

1	b	2	c	3	b	4	a	5	b
6	c	7	d	8	b	9	a	10	a
11	d	12	b	13	c	14	a	15	c
16	a	17	b	18	b	19	a	20	a
21	b	22	c	23	b	24	c	25	b
26	c	27	b	28	a	29	a	30	d
31	d								

Valve Electronics

1	c	2	c	3	a	4	b	5	b
6	b	7	c	8	b	9	a	10	a
11	c	12	b	13	b	14	c	15	d
16	b	17	b	18	c	19	c	20	c
21	b	22	b	23	b	24	c	25	a
26	c	27	d	28	a	29	a	30	ad
31	d	32	c	33	c	34	a	35	a
36	c	37	b	38	d	39	b	40	c
41	c	42	b	43	d	44	b	45	c
46	c	47	b	48	b	49	a	50	c
51	a	52	b	53	b	54	a	55	c
56	a	57	a	58	d				

Critical Thinking Questions

1	c	2	a	3	c	4	c	5	abd
6	a	7	a	8	c	9	b	10	b
11	d	12	c	13	a	14	b	15	a
16	d	17	b	18	a	19	a	20	c
21	b	22	a	23	d	24	d	25	a
26	b	27	b	28	d	29	c	30	a
31	b	32	c	33	d	34	b	35	c
36	b	37	d	38	d	39	d	40	b
41	c	42	a	43	a	44	b	45	a
46	c	47	a	48	a	49	b	50	b

Graphical Questions

1	c	2	b	3	c	4	c	5	a

6	b	7	b	8	c	9	b	10	a
11	b	12	a	13	d	14	a	15	d
16	a	17	c	18	c	19	a	20	c
21	c	22	c	23	a	24	b	25	c
26	c	27	b	28	c	29	a	30	d

Assertion and Reason

1	d	2	a	3	c	4	a	5	d
6	a	7	b	8	a	9	b	10	a
11	c	12	e	13	e	14	d	15	b
16	d	17	d	18	a	19	d	20	a
21	c	22	d	23	a	24	a	25	b
26	a	27	a	28	a	29	b	30	c
31	b								

Answers and Solutions

Solids and Crystals

1. (d) Ionic bonds cone into being when atoms that have low ionization energies, and hence lose electrons rapidly, interact with other atoms that and to acquire excess electrons. The former atoms give up electrons to the latter and they there upon become positive and negative ions respectively.

2. (d) For tetragonal, cubic and orthorhombic system $\alpha = \beta = \gamma = 90°$.

3. (d) Tourmaline crystal is biaxial.

4. (a) The temperature co-efficient of resistance of conductor is positive.

5. (a) Density $\rho = \dfrac{nA}{N(a)^3}$

where n = 2 for bcc structure , $A = 39 \times 10^{-3}$ kg,

$N = 6.02 \times 10^{23}$, $a = \dfrac{2}{\sqrt{3}}d = \dfrac{2}{\sqrt{3}} \times (4.525 \times 10^{-10})m$

(d = nearest neighbour distance = distance between centres of two neighbouring atoms $= \dfrac{a}{\sqrt{2}}$)

On putting the values we get ρ = 907

6. (a) The highest energy level which an electron can occupy in the valence band at 0 K, is called Fermi energy level.

7. (a) In a triclinic crystal $a \neq b \neq c$ and $\alpha \neq \beta \neq \gamma \neq 90°$

8. (b) Metallic solids are opaque because incident light is absorbed by the free electrons in a metal.

9. (a) In ionic bonding electrons are transferred from one type of atoms to the other type creating positive and negative ions. For example in *NaCl*, *Na* loses one electrons and *Cl* gains one so that *Na* and *Cl* ions have a stable shell structure.

10. (c) Wood is non-crystalline.

11. (d) *Cu* has *fcc* structure, for *fcc* structure co-ordination number = 12

12. (c) Vander Waal force is weak dipole-dipole interaction.

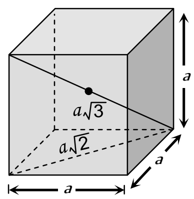
13. (b)

14. (a) The sodium chloride crystal structure has a *fcc* lattice with one chloride ion at each lattice point and one sodium ion half a cube length above it.

15. (a) In *NaCl* crystal *Na* ion is surrounded by $6\,Cl^-$ ion, therefore coordination number of *Na* is 6.

16. (a) Sodium has *bcc* structure. The distance between body centre and a corner $= \dfrac{\sqrt{3}\,a}{2}$

$= \dfrac{\sqrt{3} \times 4.225}{2} = 3.66\ \text{Å}$

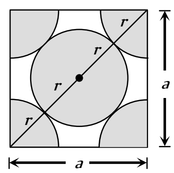


17. (d)

18. (b) For the *fcc* structure

$4r = (a^2 + a^2)^{1/2} = a\sqrt{2}$

$\Rightarrow r = \dfrac{a\sqrt{2}}{4} = \dfrac{a}{2\sqrt{2}}$



19. (c) Metals reflects incident light by the vibrations of free electrons under the influence of electric field of incident wave. The conductivity of metals decreases with increase of temperature due to increase in random motion of free electrons. The bonding is therefore metallic.

20. (c)

21. (b) The nearest distance between two atoms in a *bcc* lattice = 2 (atomic radius) $= 2 \times \left(\dfrac{\sqrt{3}\,a}{4}\right) = \dfrac{\sqrt{3}a}{2}$

22. (a) The net force on electron placed at the centre of *bcc* structure is zero. (By the principle of superposition of couloumb forces)

23. (b) For *bcc* packing, distance between two nearest atoms $d = 2r = 2\left(\dfrac{\sqrt{3}\,a}{4}\right)$

$\Rightarrow$ Lattice constant $a = \dfrac{2d}{\sqrt{3}} = \dfrac{2 \times 3.7}{\sqrt{3}} = 4.3\text{Å}$

24. (a)

25. (d) $\sqrt{2}\,a = 4r \Rightarrow a = \dfrac{4r}{\sqrt{2}} = \sqrt{2}(2r) = \sqrt{2} \times 2.54 = 3.59\ \text{Å}$

26. (d)

27. (d) Covalent bonding exists in semi-conductor.

28. (d) In H_2O covalent bonding is present.

Semiconductors

1. (c) In *P*-type semiconductors, holes are the majority charge carriers

2. (b) *Ga* has a valancy of 3.

3. (d) Ge + Trivalent impurity → P - type semiconductor

4. (b) Since $n_e > n_h$; the semiconductor is *N*-type.

5. (b) Absence of one electron, creates the positive charge of magnitude equal to that of electronic charge.

6. (b) Ge + Pantavalent impurity → N - type semiconductor

7. (b) Impurity increases the conductivity.

8. (c) Intrinsic semiconductor → Conductivity is due to the breaking of covalent bond

Extrisnsic semiconductor → Conductivity is due to the breaking of covalent bond and excess of charge carriers due to impurity.

9. (d) Resistance of conductors (Cu) decreases with decrease in temperature while that of semi-conductors (Ge) increases with decrease in temperature.

10. (a) Aluminum is trivalent impurity.

11. (b) With temperature rise conductivity of semiconductors increases.

12. (a)

13. (a) Similar to Q. 11

14. (d) In insulators, the forbidden energy gap is largest and it is of the order of 6 eV.

15. (c) N-type semiconductors are neutral because neutral atoms are added during doping.

16. (b)

17. (b) In insulators, the forbidden energy gap is very large, in case of semiconductor it is moderate and in conductors the energy gap is zero.

18. (b) Similar to Q. 15.

19. (c) Phosphorus is pentavalent.

20. (c) In intrinsic semiconductors, the creation or liberation of one free electron by the thermal energy has created one hole. Thus in intrinsic semiconductors $n_e = n_h$

21. (d) Conductor has positive temperature coefficient of resistance but semiconductor has negative temperature coefficient of resistance.

22. (b) Boron is trivalent.

23. (a, c) In intrinsic semiconductors, electrons and holes both are charge carriers. In P-type semiconductors (Extrinsic semiconductors) holes are majority charge carriers.

24. (d)

25. (b)

26. (c) $\Delta E_{g(Germanium)} = 0.67\ eV$

27. (d) In P-type semiconductors, holes are majority charge carrier and electrons are minority charge carriers.

28. (c) At zero Kelvin, there is no thermal agitation and therefore no electrons from valence band are able to shift to conduction band.

29. (c) Antimony is a fifth group impurity and is therefore a donor of electrons.

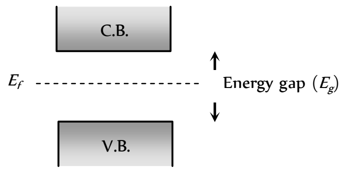
30. (b) Resistance of semiconductor $\propto \frac{1}{\text{Temperature}}$

31. (d) Extrinsic S.C. → $P - \text{Type}\,(n_p >> n_e)$; → $N - \text{Type}\,(n_e >> n_p)$

32. (a) At room temperature the number of electrons and holes are equal in the intrinsic semiconductor.

33. (b) Indium is trivalent, hence on doping with it, the intrinsic semiconductor becomes P-type semiconductor.

34. (a)



35. (c) In semiconductors, Forbidden energy gap is of the order of 1 eV.

36. (d) At $0K$ temperature semiconductor behaves as an insulator, because at very low temperature electrons cannot jump from the valence band to conduction band.

37. (c) Antimony is pentavalent.

38. (b) At $0K$ semiconductor behaves as insulator so it's resistance is infinite.

39. (d) The conduction and valence bands in the conductors merge into each other.

40. (a) For N-type semiconductor, the impurity should be pentavalent.

41. (d) When a free electron is produced, simultaneously a hole is also produced.

42. (c) For P – type semiconductor the doping impurity should be trivalent.

43. (b) The temperature co-efficient of resistance of a semiconductor is always negative.

44. (c) The resistance of semiconductor decreases with the increase in temperature.

45. (d) At absolute zero temperature, semiconductor.

46. (b) Formation of energy bands in solids are due to Pauli's exclusion principle.

47. (a) In P-type semiconductors, holes are majority charge carriers.

48. (b)

49. (a) Conductivity of semiconductors increases with rise in temperature.

50. (d) All are trivalent in nature.

51. (d) In N-type semiconductors, electrons are majority charge corners.

52. (b) When a strong current passes through the semiconductor it heats up the crystal and covalent bond are broken. Hence because of excess number of free electrons it behaves like a conductor.

53. (b)

54. (a) Phosphorus is a pentavalent impurity so $n_e > n_h$.

55. (c) Phosphorus is pentavalent while Indium is trivalent.

56. (d) Phosphorus and Arsenic both are pentavalent.

57. (b)

58. (d)

59. (a) For Ge, $E_g = 0.7\,eV = 0.7 \times 1.6 \times 10^{-19}\,J = 1.12 \times 10^{-19}\,J$

60. (a) At room temperature some covalent bond breaks and semiconductor behaves slightly as a conductor.

61. (b)

62. (a)

63. (c) Because boron is a trivalent impurity.

64. (a) In P-type semi conductor, holes are majority charge carriers.

65. (b) In intrinsic semiconductors, at room temperature $n_e = n_h$.

66. (a) In conductors valence band and conduction band overlaps.

67. (c) Because As is pentavalent impurity.

68. (c) At 0 K semiconductor behaves as an insulator.

69. (c)

70. (c)

71. (b) Antimony and phosphorous both are pentavalent.

72. (b) Gallium is trivalent impurity.

73. (a)

74. (b) One atom of pentavalent impurity, donates one electron.

75. (c)

76. (b) The charge on hole is positive.

77. (c) Phosphorus is pentavalent impurity.

78. (a) $n_i^2 = n_h n_e \Rightarrow (10^{19})^2 = 10^{21} \times n_e \Rightarrow n_e = 10^{17} / m^3$.

79. (d) Temperature co-efficient of semiconductor is negative.

80. (a) Copper, Aluminum, Iron are conductors, while Ge is semiconductor.

81. (a) At room temperature, few bonds breaks and electron hole pair generates inside the semiconductor.

82. (a)

83. (b) With rise in temperature, conductivity of semiconductor increases while resistance decreases.

84. (d) Gallium, boron and aluminum are trivalent.

85. (c) Because with rise in temperature, resistance of semiconductor decreases, hence overall resistance of the circuit increases, which in turn increases the current in the circuit.

86. (d) Extrinsic semiconductor (N-type or P-type) are neutral.

87. (a) Because $v_d = \dfrac{i}{(n_e)eA}$

88. (c)

89. (b) Resistivity is the intrinsic property, it doesn't depend upon length and shape of the semiconductors.

90. (c)

91. (a) $\lambda_{max} = \dfrac{hc}{E} = \dfrac{6.6 \times 10^{-34} \times 3 \times 10^8}{1.14 \times 1.6 \times 10^{-19}} = 10888 Å$

92. (b) In N-type semiconductor impurity energy level lies just below the conduction band.

93. (d)

94. (d)

95. (d) $\sigma = en_e \mu_e$

$$\Rightarrow n_e = \frac{\sigma}{e\mu_e} = \frac{6.24}{1.6 \times 10^{-19 \times 3900}} = 10^{16} / cm^3$$

96. (d) In semiconductors, the forbidden energy gap between the valence band and conduction band is very small, almost equal to kT. Moreover, valence band is completely filled where as conduction band is empty.

97. (d) In sample x no impurity level seen, so it is undoped. In sample y impurity energy level lies below the conduction bond so it is doped with fifth group impurity.

In sample z, impurity energy level lies above the valence band so it is doped with third group impurity.

98. (a) Forbidden energy gap for carbon is greater than that of silicon.

99. (b)

100. (a) Because electrons needed less energy to move.

101. (b)

Semiconductor Diode

1. (b)

2. (a) In forward biased *PN*-junction, external voltage decreases the potential barrier, so current is maximum. While in reversed biased *PN*-junction, external voltage increases the potential barrier, so the current is very small.

3. (b)

4. (b) Filter circuits are used to get smooth *dc* π -filter is the best filter.

5. (c) In reverse bias no current flows.

6. (b) In reverse biasing, width of depletion layer increases.

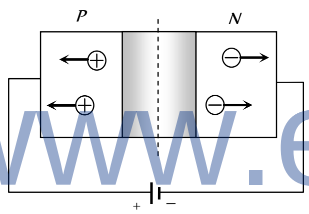
7. (a) Depletion layer consist of mainly stationary ions.

8. (b) Current flow is possible and $i = \frac{V}{R} = \frac{(4-1)}{300} = 10^{-2} A$

9. (a) The potential of *P*-side is more negative that of *N*-side, hence diode is in reverse biasing. In reverse biasing it acts as open circuit, hence no current flows.

10. (a)

11. (b) It is used to convert *ac* into *dc* (rectifier)



12. (b)

13. (b) Because in case (1) N is connected with N. This is not a series combination of transistor.

14. (c)

15. (d)

16. (c) After a large reverse voltage is *PN*-junction diode, a huge current flows in the reverse direction suddenly. This is called Breakdown of *PN*-junction diode.

17. (c) In forward biasing both positive and negative charge carriers move towards the junction.

18. (b,c)

19. (c) When polarity of the battery is reversed, the *P-N* junction becomes reverse biased so no current flows.

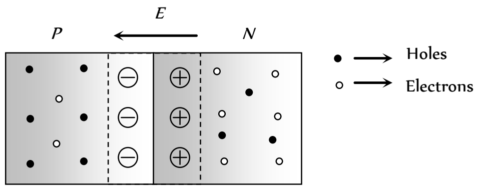
20. (d) Resistance in forward biasing $R_{fr} \approx 10\,\Omega$ and resistance in reverse biasing $R_{Rw} \approx 10^5 \Omega \Rightarrow \frac{R_{fr}}{R_{Rw}} = \frac{1}{10^4}$

21. (d)

22. (b) In forward biasing width of depletion layer decreases.

23. (d)

24. (c) At junction a potential barrier/depletion layer is formed, with *N*-side at higher potential and *P*-side at lower potential. Therefore there is an electric field at the junction directed from the *N*-side to *P*-side



25. (c) In *N*-type semiconductor majority charge carriers are electrons.

26. (b) In forward biasing the diffusion current increases and drift current remains constant so not current is due to the diffusion.

In reverse biasing diffusion becomes more difficult so net current (very small) is due to the drift.

27. (b) At a particular reverse voltage in *PN*-junction, a huge current flows in reverse direction known as avalanche current.

28. (b) Due to the large concentration of electrons in *N*-side and holes in *P*-side, they diffuses from their own side to other side. Hence depletion region produces.

29. (c) Only in option (c), *P*-side is more negative as compared to *N*-side.

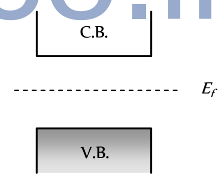
30. (b) Depletion layer is more in less doped side.

31. (b) In forward biasing *P*-side is connected with positive terminal and *N*-side with negative terminal of the battery

32. (c) In forward biasing of *PN*-junction diode, current mainly flows due to the diffusion of majority charge carriers.

33. (d)

34. (c) In forward biasing of *PN* junction diode width of depletion layer decreases. In intrinsic semiconductor fermi energy level is exactly in the middle of the forbidden gap



35. (d)

36. (a) At high reverse voltage, the minority charge carriers, acquires very high velocities. These by collision break down the covalent bonds, generating more carriers. This mechanism is called Avalanche breakdown.

37. (b) Because *P*-side is more negative as compared to *N*-side.

38. (b) When reverse bias is increased, the electric field at the junction also increases. At some stage the electric field breaks the covalent bond, thus the large number of charge carriers are generated. This is called Zener breakdown.

39. (d) In forward biasing both V, and x decreases.

40. (a)

41. (b) In figure 2,4 and 5. *P*-crystals are more positive as compared to *N*-crystals.

42. (a) *ac* → Rectifier → *dc*

43. (b) In this condition $P - N$ junction is reverse biased.

44. (a)

45. (a) $E = \frac{V}{d} = \frac{0.5}{5 \times 10^{-7}} = 10^6 \; V/m$.

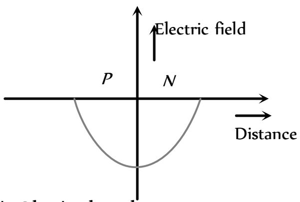
46. (b) Across the $P-N$ junction, a barrier potential is developed whose direction is from N region to P region.

47. (b)

48. (a) In forward biasing, resistance of PN junction diode is zero, so whole voltage appears across the resistance.

49. (c)

50. (d) The electric field strength versus distance curve across the *P-N* junction is as follows



51. (d)

52. (a) It doesn't Obey's ohms law.

53. (c) Because *N*-side is more positive as compared to *P*-side.

54. (c) When a light (wavelength sufficient to break the covalent bond) falls on the junction, new hole electron pairs are created. No. of produced electron hole pair deponed upon no. of photons. So photo emf or current proportional to intensity of light.

55. (b)

56. (d) For full wave rectifier $\eta = \dfrac{81.2}{1+\dfrac{r_f}{R_L}}$

$\Rightarrow \eta_{max} = 81.2\%$ $\quad (r_f << R_L)$

57. (a)

58. (a)

59. (c) In reverse biasing negative terminal of the battery is connected to *N*-side.

60. (a) In the given condition diode is in reverse biasing so it acts as open circuit. Hence potential difference between *A* and *B* is 6 *V*

61. (b) Zener breakdown can occur in heavily doped diodes. In lightly doped diodes the necessary voltage is higher, and avalanche multiplication is then the chief process involved.

62. (c)

63. (a)

64. (c) Diode acts as open switch only when it is reverse biased

65. (a) Because *P*-side is more negative than *N*-side.

66. (b) In unbiased condition of *PN*-junction, depletion region is generated which stops the movement of charge carriers.

67. (c) For a wide range of values of load resistance, the current in the zener diode may change but the voltage across it remains unaffected. Thus the output voltage across the zener diode is a regulated voltage.

68. (c)

69. (d) Arsenic has five valence electrons, so it a donor impurity. Hence *X* becomes *N*-type semiconductor. Indium has only three outer electrons, so it is an acceptor impurity. Hence *Y* becomes *P*-type semiconductor. Also *N* (*i.e. X*) is connected to positive terminal of battery and *P*(*i.e. Y*) is connected to negative terminal of battery so *PN*-junction is reverse biased.

70. (a)

71. (c) In photodiode, it is illuminated by light radiations, which in turn produces electric current.

72. (a)

73. (d)

74. (d) By using $E = \dfrac{V}{d} = \dfrac{0.6}{10^{-6}} = 6\times10^{5}\ V/m$

75. (c) The given circuit is full wave rectifier.

76. (a) The diode is in reverse biasing so current through it is zero.

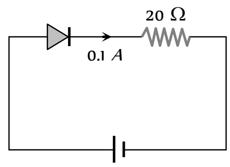
77. (c) In full wave rectifier, the fundamental frequency in ripple is twice that of input frequency.

78. (c)

79. (c) $V' = V + IR$

$= 0.5 + 0.1 \times 20$

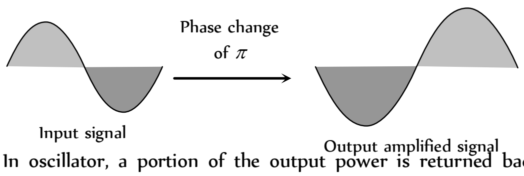
$= 2.5\ V$



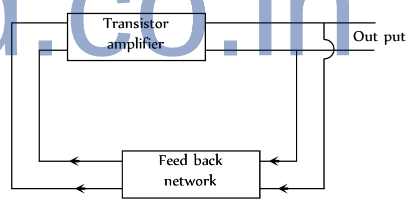
Junction Transistor

1. (a) When *NPN* transistor is used as an amplifier, majority charge carrier electrons of *N*-type emitter move from emitter to base and than base to collector.

2. (c)



3. (a) In oscillator, a portion of the output power is returned back (feed back) to the input in phase with the starting power. This process is termed as positive feedback.

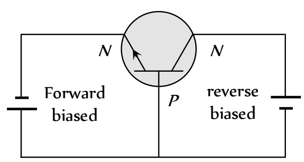


4. (d) The emitter base junction is forward biased while collector base junction is reversed biased.

5. (d) Given $i_c = \dfrac{80}{100}\times i_e \Rightarrow 24 = \dfrac{80}{100}\times i_e \Rightarrow i_e = 30\,mA$

By using $i_e = i_b + i_c \Rightarrow i_b = 30 - 24 = 6\ mA$.

6. (b)



7. (d) α is the ratio of collector current and emitter current while β is the ratio of collector current and base current.

8. (b)

9. (b) $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.98}{1-0.98} = 49.$

10. (b) $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.96}{1-0.96} = 24.$

11. (c) $\alpha = \frac{i_c}{i_e}$ = 0.96 and i_e = 7.2 mA

$\Rightarrow i_c = 0.96 \times i_e$ = 0.96 × 7.2 = 6.91 mA

$\therefore i_e = i_c + i_b \Rightarrow$ 7.2 = 6.91 + $i_b \Rightarrow i_b$ = 0.29 mA.

12. (d)

13. (d) $i_C = \frac{90}{100} \times i_E \Rightarrow$ 10 = 0.9 × i_E = 11mA

Also $i_E = i_B + i_C \Rightarrow i_B = 11 - 10 = 1mA$.

14. (a) Current gain $\beta = \frac{\Delta i_c}{\Delta i_b} \Rightarrow \Delta i_c = \beta \times \Delta i_b$ = 80 × 250 μA.

15. (b) In transistor, base is least doped.

16. (b)

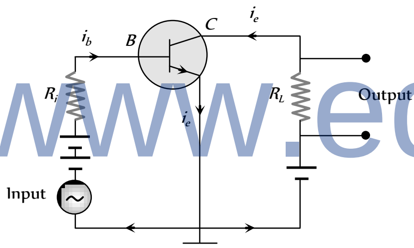
17. (d) β = 50, R_i = 1000 Ω, V_i = 0.01 V

$\beta = \frac{i_c}{i_b}$ and $i_b = \frac{V_i}{R_i} = \frac{0.01}{10^3} = 10^{-5} A$

Hence $i_c = 50 \times 10^{-5} A = 500 \mu A$.

18. (b) $\alpha = \frac{\beta}{1+\beta} = \frac{99}{1+99} = 0.99$.

19. (a,c) The circuit of a CE amplifier is as shown below.



This has been shown a NPN transistor. Therefore base emitter are forward, biased and input signal is connected between base and emitter.

20. (a) The base is always thin

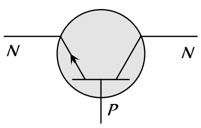
21. (c) Voltage gain = β × Resistance gain

$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{(1-0.99)} = 99$

Resistance gain $= \frac{10 \times 10^3}{10^3} = 10$

$\Rightarrow$ Voltage gain = 99 × 10 = 990.

22. (a) The arrow head in the transistor symbol always shows the direction of hole flow in the emitter region.



23. (b)

24. (b) Because emitter (N) is common to both, base (P) and collector (N).

25. (b) Emitter is heavily doped.

26. (c) α = 0.8 $\Rightarrow \beta = \frac{0.8}{(1-0.8)}$ = 4

Also $\beta = \frac{\Delta i_c}{\Delta i_b} \Rightarrow \Delta i_c = \beta \times \Delta i_b$ = 4 × 6 = 24mA.

27. (a) $\Delta i_c = \alpha \, \Delta i_e = 0.98 \times 2 = 1.96 \, mA$

$\therefore \quad \Delta i_b = \Delta i_e - \Delta i_c = 2 - 1.96 = 0.04 \, mA$.

28. (b) $i_e = i_b + i_c \Rightarrow i_c = i_e - i_b$

29. (b) $V_b = i_b R_b \Rightarrow R_b = \frac{9}{35 \times 10^{-6}}$ = 257 $k\Omega$.

30. (d) $\Delta i_e = \Delta i_c + \Delta i_b$

$\Rightarrow$ 8 = 7.8 + $\Delta i_b \Rightarrow \Delta i_b$ = 0.2mA = 200 μA.

31. (b) $\beta = \frac{i_c}{i_b}$

32. (b) FET is unipolar.

33. (a)

34. (b) $i_e = i_b + i_c \Rightarrow \frac{i_e}{i_c} = \frac{i_b}{i_c} + 1 \Rightarrow \frac{1}{\alpha} = \frac{1}{\beta} + 1 \Rightarrow \alpha = \frac{\beta}{(1+\beta)}$.

35. (b) In NPN transistor when emitter-base is forward biased, electrons move from emitter to base.

36. (a) Here $\Delta V_c = 0.5 \, V$, Δi_c = 0.05mA = 0.05 × $10^{-3} A$

Output resistance is given by

$R_{out} = \frac{\Delta V_c}{\Delta i_c} = \frac{0.5}{0.05 \times 10^{-3}} = 10^4 \Omega$ = 10$k\Omega$.

37. (a) Oscillator can produce radio waves of constant amplitude.

38. (a) $h_{fe} = \left(\frac{\Delta i_c}{\Delta i_b}\right)_{V_{ce}} = \frac{8.2}{8.3 - 8.2} = 82$

39. (b) Current gain $\beta = \frac{\Delta i_c}{\Delta i_b} \Rightarrow \Delta i_b = \frac{1 \times 10^{-3}}{100} = 10^{-5} A$ = 0.01mA.

By using $\Delta i_e = \Delta i_b + \Delta i_c \Rightarrow \Delta i_e$ = 1.01 + 1 = 1.01mA.

40. (a) In CB amplifier Input and output voltage signal are in same phase.

41. (b)

42. (d)

43. (d) For CE configuration voltage gain $= \beta \times R_L / R_i$

Power gain $= \beta^2 \times R_L / R_i \Rightarrow \frac{\text{Power gain}}{\text{Voltage gain}} = \beta$

44. (b) As we know $i_E = i_C + i_B$

$\Rightarrow \frac{i_e}{i_c} = 1 + \frac{i_b}{i_c} \Rightarrow \frac{1}{\alpha} = 1 + \frac{1}{\beta} \Rightarrow \beta = \frac{\alpha}{1-\alpha}$.

Digital Electronics

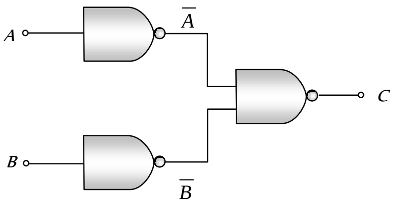
1. (b)

2. (c)

3. (b) For 'OR' gate $X = A + B$

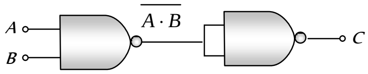
i.e. $0+0=0$, $0+1=1$, $1+0=1$, $1+1=1$

4. (a)



$C=\overline{\overline{A}.\overline{B}}=\overline{\overline{A}}+\overline{\overline{B}}=A+B$ (De morgan's theorem)

Hence output C is equivalent to OR gate.



$C=\overline{\overline{AB}.\overline{AB}}=\overline{\overline{AB}}+\overline{\overline{AB}}=AB+AB=AB$

In this case output C is equivalent to AND gate.

5. (b) In 'NOR' gate $Y=\overline{A+B}$

i.e. $\overline{0+0}=\overline{0}=1$, $\overline{1+0}=\overline{1}=0$

$\overline{0+1}=\overline{1}=0$, $\overline{1+1}=\overline{1}=0$

6. (c) For 'XNOR' gate $Y=\overline{A}\,\overline{B}+AB$

i.e. $\overline{0}.\overline{0}+0.0=1.1+0.0=1+0=1$

$\overline{0}.\overline{1}+0.1=1.0+0.1=0+0=0$

$\overline{1}.\overline{0}+1.0=0.1+1.0=0+0=0$

$\overline{1}.\overline{1}+1.1=0.0+1.1=0+1=1$

7. (d) The output D for the given combination

$D=\overline{(A+B).C}=\overline{(A+B)}+\overline{C}$

If $A=B=C=0$ then $D=\overline{(0+0)}+\overline{0}=\overline{0}+\overline{0}=1+1=1$

If $A=B=1, C=0$ then $D=\overline{(1+1)}+\overline{0}=\overline{1}+\overline{0}=0+1=1$

8. (b)

9. (a) The Boolean expression for 'NOR' gate is $Y=\overline{A+B}$

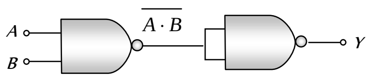
i.e. if $A=B=0$ (Low), $Y=\overline{0+0}=\overline{0}=1$ (High)

10. (a)

11. (d) The Boolean expression for 'AND' gate is $R=P.Q$

$\Rightarrow 1.1=1,\ 1.0=0,\ 0.1=0,\ 0.0=0$

12. (b) Two 'NAND' gates are required as follows



$Y=\overline{\overline{AB}.\overline{AB}}=AB$

13. (c) For 'NAND' gate (option c), output $=\overline{0.1}=\overline{0}=1$

14. (a) AND + NOT $\rightarrow$ NAND

15. (c) For 'NOT' gate $X=\overline{A}$

16. (a) The given Boolean expression can be written as

$Y=\overline{(A+B)}.\overline{(A.B)}=(\overline{A}.\overline{B}).(\overline{A}+\overline{B})=(\overline{A}\,\overline{A}).\overline{B}+\overline{A}(\overline{B}.\overline{B})$

$=\overline{A}.\overline{B}+\overline{A}\,\overline{B}=\overline{A}\,\overline{B}$

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

17. (b) For 'AND' gate, if output is 1 then both inputs must be 1.

18. (b)

19. (a)

20. (a) The given symbol is of 'AND' gate.

21. (b) It is the symbol of 'NOR' gate.

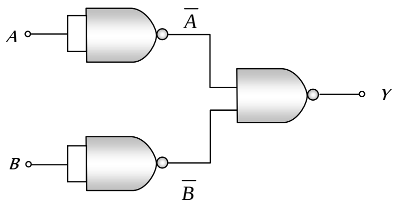
22. (c) The Boolean expression for the given combination is output $Y=(A+B).C$

The truth table is

A	B	C	Y =(A+B).C
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
0	1	1	1
1	0	1	1
1	1	1	1

Hence $A=1$, $B=0$, $C=1$

23. (b)



$Y=\overline{\overline{A}.\overline{B}}=\overline{\overline{A}}+\overline{\overline{B}}=A+B$

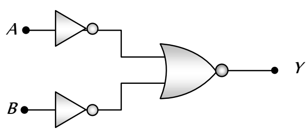
This output equation is equivalent to OR gate.

24. (c) If inputs are A and B then output for NAND gate is $Y=\overline{AB}$

$\Rightarrow$ If $A=B=1$, $Y=\overline{1.1}=\overline{1}=0$

25. (b)

26. (c)



$Y=\overline{\overline{A}+\overline{B}}$

According to De morgan's theorem

$Y=\overline{\overline{A}+\overline{B}}=\overline{\overline{A}}.\overline{\overline{B}}=A.B$

This is the output equation of 'AND' gate.

27. (b) The output of OR gate is $Y = A + B$.

28. (a) The given symbol is of NAND gate.

29. (a) $(100010)_2 = 2^5 \times 1 + 2^4 \times 0 + 2^3 \times 0 + 2^2 \times 0 +$

$$2^1 \times 1 + 2^0 \times 0 = 32 + 0 + 0 + 0 + 2 + 0 = (34)_{10}$$

and $(11011)_2 = 2^4 \times 1 + 2^3 \times 1 + 2^2 \times 0 + 2^1 \times 1 + 2^0 \times 1$

$$= 16 + 8 + 0 + 2 + 1 = (27)_{10}$$

$\therefore$ Sum $(100010)_2 + (11011)_2 = (34)_{10} + (27)_{10} = (61)_{10}$

Now

2	61	Remainder
2	30	1 LSD
2	15	0
2	7	1
2	3	1
2	1	1
	0	1 MSD

$\therefore$ Required sum (in binary system)

$(100010)_2 + (11011)_2 = (111101)_2$

30. (d) For 'NAND' gate $C = \overline{A.B}$

i.e. $\overline{0.0} = \overline{0} = 1$, $\overline{0.1} = \overline{0} = 1$

$\overline{1.0} = \overline{0} = 1$, $\overline{1.1} = \overline{1} = 0$

31. (d) 'NOR' gates are considered as universal gates, because all the gates like AND, OR, NOT can be obtained by using only NOR gates.

Valve Electronics (Diode and Triode)

1. (c) According to Richardson-Dushman equation, number of thermions emitted per sec per unit area $J = AT^2 e^{-W_0/kT} \Rightarrow J \propto T^2$

2. (c) Intensity $\propto$ Number of electrons

3. (a) In SCR (Space charge region) electrons collect around the plate, this cloud decreases the emission of electrons from the cathode, hence plate current decreases.

4. (b)

5. (b) By using $g_m = \frac{\Delta i_p}{\Delta v_g} \Rightarrow 3 \times 10^{-4} = \frac{\Delta i_p}{-1-(-3)}$

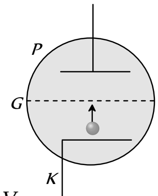
$$\Rightarrow \Delta i_p = 6 \times 10^{-4} A = 0.6\, mA$$

6. (b) Voltage gain $A_v = \frac{\mu}{1 + \frac{r_p}{R_L}}$ and $\mu = r_p \times g_m$

$$\Rightarrow r_p = \frac{42}{2 \times 10^{-3}} = 21000\,\Omega \Rightarrow A_v = \frac{42}{1 + \frac{21000}{50 \times 10^3}} = 29.57$$

7. (c) Voltage gain $A_v = \frac{\mu}{1 + \frac{r_p}{R_L}}$, for $r_p = R_L \Rightarrow A_v = \frac{\mu}{2}$

8. (b) When grid is given positive potential more electrons will cross the grid to reach the positive plate *P*. Hence current increases.



9. (a) By using $\mu = -\frac{\Delta V_p}{\Delta V_g} = r_p \times g_m$

$$\Rightarrow 7 \times 10^3 \times 2.5 \times 10^{-3} = -\frac{50}{\Delta V_g} \Rightarrow \Delta V_g = -2.86\,V.$$

10. (a) Using voltage gain $A_v = \frac{\mu}{1 + \frac{r_p}{R_L}}$ also $\mu = r_p \times g_m$

$$\Rightarrow r_p = \frac{\mu}{g_m} = \frac{20}{3 \times 10^{-3}}$$

$$\therefore A_v = \frac{20}{1 + \frac{20}{3 \times 10^{-3} \times 3 \times 10^4}} = \frac{180}{11} = 16.36.$$

11. (c) Voltage gain $= \frac{V_{out}}{V_{in}} = \frac{\mu}{1 + \frac{r_p}{R_L}} \Rightarrow \frac{V_{out}}{0.5} = \frac{25}{1 + \frac{40 \times 10^3}{10 \times 10^3}}$

$$\Rightarrow V_{out} = 2.5\,V.$$

12. (b) $\mu = -\frac{\Delta V_p}{\Delta V_G} \Rightarrow \Delta V_p = -\mu \Delta V_G = -20 \times (-0.2) = 4\,V$.

13. (b) Voltage gain $A_V = \frac{\mu}{1 + \frac{r_p}{R_L}}$ and $\mu = r_p \times g_m$

$$\Rightarrow \mu = 10 \times 10^3 \times 3 \times 10^{-3} = 30$$

$$\therefore A_v = \frac{\mu}{1 + \frac{r_p}{2r_p}} = \frac{2}{3}\mu = \frac{2}{3} \times 30 = 20.$$

14. (c)

15. (d) After saturation plate current can be increased by increasing the temperature of filament. It can be done by increasing the filament current.

16. (b) The maximum voltage gain $(A)_{max} = \mu$

(Which is obtained when $R_L = \infty$).

17. (b) Voltage gain $A_v = \frac{\mu}{1 + \frac{r_p}{R_L}}$

$$\because R_L = 1.5 r_p \Rightarrow A_v = \frac{\mu}{1 + \frac{r_p}{1.5 r_p}} = \frac{3}{5}\mu = \frac{3}{5} \times 20 = 12.$$

18. (c)

19. (c)

20. (c) $\mu = \frac{\Delta V_p}{\Delta V_g} \Rightarrow \Delta V_p = \mu \Delta V_g = 15 \times 0.3 = 4.5$ *volt*.

21. (b) Plate resistance $=\frac{1}{\text{slope}}=\frac{1}{10^{-3}\times10^{-3}}=10^6\Omega$

$=1000\ k\Omega$ (static).

22. (b) Using $A_v=\frac{\mu}{1+\frac{r_p}{R_L}}$ and $\mu=r_p\times g_m$

$$\Rightarrow r_p=\frac{\mu}{g_m}=\frac{50}{2\times10^{-3}}=25\times10^3\Omega$$

$$\therefore A_v=\frac{50}{1+\frac{25\times10^3}{25\times10^3}}=25.$$

23. (b) $P=Vi\Rightarrow V=\frac{P}{i}=\frac{448\times10^{-3}}{14\times10^{15}\times1.6\times10^{-19}}=200V$

24. (c) $\mu=\frac{(V_{P_1}-V_{P_2})}{(V_{G_1}-V_{G_2})}=\frac{(200-220)}{(0.5-1.3)}=25.$

25. (a) $\mu=r_p\times g_m\Rightarrow g_m=\frac{\mu}{r_p}=\frac{22}{6600}=\frac{1}{300}.$

26. (c) $r_p=\frac{V_{P_1}-V_{P_2}}{I_{P_1}-I_{P_2}}=\frac{75-100}{(2-4)\times10^{-3}}=12.5\times10^3\Omega=12.5k\Omega.$

27. (d)

28. (a)

29. (a) Voltage amplification $A_v=\frac{\mu}{1+\frac{r_p}{R_L}}$

$$\Rightarrow 25=\frac{\mu}{1+\frac{r_p}{50\times10^3}}\quad......(i)$$

and $$30=\frac{\mu}{1+\frac{r_p}{100\times10^3}}\quad......(ii)$$

an solving equation (i) and (ii), $r_p=25k\Omega$.

30. (a, d)

31. (d)

32. (c) Before saturation region, linear region comes. In linear region $i_p\propto V_p$

$$\Rightarrow\frac{i_1}{i_2}=\frac{V_{P_1}}{V_{P_2}}=\frac{400}{200}=\frac{2}{1}.$$

33. (c) $i=1.125-1.112=0.013A=13\ mA$.

34. (a)

35. (a)

36. (c) Comparing the given equation with standard equation

$$i=AT^2e^{qV/kT}\Rightarrow V_L=\frac{kT}{V}.$$

37. (b)

38. (d) $r_p=\frac{\Delta V_p}{\Delta i_p}=\frac{150-100}{(12-7.5)\times10^{-3}}=\frac{50}{4.5}\times10^3=11.1k\Omega.$

39. (b)

40. (c) Voltage amplification $A_v=\frac{\mu}{1+\frac{r_p}{R_L}}=\frac{\mu R_L}{R_L+r_p}$

$$\Rightarrow\frac{A_1}{A_2}=\frac{2+4}{4+4}=\frac{3}{4}.$$

41. (c) A diode is used as a rectifier to convert *ac* in to *dc*.

42. (b) Fluctuating *dc* → Filter circuit → smooth *dc*.

43. (d)

44. (b)

45. (c) $\mu=r_p\times g_m\Rightarrow r_p=\frac{20}{10^{-3}}=2\times10^4\Omega.$

46. (c)

47. (b) $\mu=-\frac{\Delta V_p}{\Delta V_g}$

$$\Rightarrow\Delta V_p=-\mu\times\Delta V_g=-50(-0.20)=10\ V.$$

48. (b) $r_p=\frac{1}{\text{slope}}=\frac{1}{2\times10^{-2}\times10^{-3}}=50k\Omega.$

49. (a) Voltage amplification $A_v=\frac{\mu}{1+\frac{r_p}{R_L}}=\frac{r_p\times g_m\times R_L}{R_L+r_p}$

$$\Rightarrow10=\frac{20\times10^3\times2.5\times10^{-3}\times R_L}{(R_L+20\times10^3)}\Rightarrow R_L=5k\Omega.$$

50. (c) Voltage gain $A_v=\frac{\mu}{1+\frac{r_p}{R_L}}=\frac{18}{1+\frac{8\times10^3}{10^4}}=10.$

51. (a) Ripple factor $r=\sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2-1}=\sqrt{\frac{(I_0/2)^2}{(I_0/\pi)^2}-1}=1.21.$

52. (b)

53. (b)

54. (a) $\mu=r_p\times g_m=2.5\times10^4\times2\times10^{-3}=50.$

55. (c) $\mu=\left(\frac{\Delta V_p}{\Delta V_g}\right)_{i_p=\text{constant}}=\frac{(225-200)}{(5.75-5)}=33.3$

56. (a) $g_m=\left(\frac{\Delta I_p}{\Delta V_g}\right)_{V_p=\text{constant}}=\frac{(7.5-5.5)}{-1.2-(-2.2)}=2m\ mho$

57. (a)

58. (d) Using $\mu=r_p\times g_m\Rightarrow g_m=\frac{20}{10\times10^3}=2\times10^{-3}.$

Critical Thinking Questions

1. (c) Number density of atoms in silicon specimen $=5\times10^{28}$ *atom/m*^{3} $=5\times10^{22}$ *atom/cm*^{3}

Since one atom of indium is doped in 5×10^7 *Si* atom. So number of indium atoms doped per *cm*^{3} of silicon.

$$n=\frac{5\times10^{22}}{5\times10^7}=1\times10^{15}\ atom/cm^3.$$

2. (a) The probability of electrons to be found in the conduction band of an intrinsic semiconductor

$$P(E)=\frac{1}{1+e^{\frac{(E-E_F)}{kT}}}$$; where k = Boltzmann's constant

Hence, at a finite temperature, the probability decreases exponentially with increasing band gap.

3. (c) When donor impurity (+5 valence) added to a pure silicon (+4 valence), the +5 valence donor atom sits in the place of + 4 valence silicon atom. So it has a net additional + 1 electronic charge. The four valence electron form covalent bond and get fixed in the lattice. The fifth electron (with net – 1 electronic charge) can be approximated to revolve around + 1 additional charge. The situation is like the hydrogen atom for which energy is given by $E=-\frac{13.6}{n^2}eV$. For the case of hydrogen, the permittivity was taken as ε_0. However, if the medium has a permittivity ε_r relative to ε_0 then $E=-\frac{13.6}{\varepsilon_r^2 n^2}eV$

For *Si*, ε_r = 12 and for n = 1, $E \simeq 0.1\,eV$

4. (c) The forward current

$$i=i_s(e^{eV/kT}-1)=10^{-5}\left[e^{\frac{1.6\times10^{-19}\times0.2}{1.4\times10^{-23}\times300}}-1\right]$$

$$=10^{-5}[2038.6-1]=20.376\times10^{-3}A$$

5. (a,b,d) At 0 *K*, a semiconductor becomes a perfect insulator. Therefore at 0 *K*, if some potential difference is applied across an insulator or a semiconductor, current is zero. But a conductor will become a superconductor at 0 *K*. Therefore, current will be infinite. In reverse biasing at 300 *K* through a *P-N* junction diode, a small finite current flows due to minority charge carriers.

6. (a) Since diode in upper branch is forward biased and in lower branch is reversed biased. So current through circuit $i=\frac{V}{R+r_d}$; here r_d = diode resistance in forward biasing = 0

$$\Rightarrow\ i=\frac{V}{R}=\frac{2}{10}=0.2A.$$

7. (a) The voltage drop across resistance = 8 – 0.5 = 7.5 *V*

$\therefore$ Current $i=\frac{7.5}{2.2\times10^3}=3.4\,mA$

8. (c) $E=\frac{hc}{\lambda}\Rightarrow\lambda=\frac{hc}{E}=\frac{6.6\times10^{-34}\times3\times10^8}{57\times10^{-3}\times1.6\times10^{-19}}$ =217100Å.

9. (b) The diode in lower branch is forward biased and diode in upper branch is reverse biased

$$\therefore\quad i=\frac{5}{20+30}=\frac{5}{50}A.$$

10. (b) The current through circuit $i=\frac{P}{V}=\frac{100\times10^{-3}}{0.5}=0.2A$

$\therefore$ voltage drop across resistance = 1.5 – 0.5 = 1 *V*

$$\Rightarrow R=\frac{1}{0.2}=5\,\Omega.$$

11. (d) In common emitter configuration current gain

$$A_i=\frac{-h_{fe}}{1+h_{oe}R_L}=\frac{-50}{1+25\times10^{-6}\times10^3}=-48.78.$$

12. (c) Voltage gain $=\frac{\text{Output voltage}}{\text{Input voltage}}$

$\Rightarrow V_0 = V_i \times$ Voltage gain

$\Rightarrow V_0 = V_i \times$ Current gain $\times$ Resistance gain

$$=V_i\times\beta\times\frac{R_L}{R_{BE}}=10^{-3}\times100\times\frac{10}{1}=1V.$$

13. (a) $n_e=8\times10^{18}/m^3,\ n_h=5\times10^{18}/m^3$

$$\mu_e=2.3\frac{m^2}{volt-sec},\ \mu_h=0.01\frac{m^2}{volt-sec}$$

$\because n_e>n_h$ so semiconductor is *N*-type

Also conductivity $\sigma=\frac{1}{\text{Resistivity}(\rho)}=e(n_e\mu_e+n_h\mu_h)$

$$\Rightarrow\frac{1}{\rho}=1.6\times10^{-19}[8\times10^{18}\times2.3+5\times10^{18}\times0.01]$$

$\Rightarrow \rho$ = 0.34 Ω-*m*.

14. (b) $V_{rms}=\frac{V_0}{2}=\frac{200}{2}=100V$

15. (a) At knee point voltage across the diode is 0.7 *V*.

Hence voltage across resistance *R* is 5 – 0.7 = 4.3 *V*.

$\Rightarrow$ using $V = iR \Rightarrow 4.3 = 1\times10^{-3}\times R \Rightarrow R = 4.3\ k\Omega$.

16. (d) In positive half cycle one diode is in forward biasing and other is in reverse biasing while in negative half cycle their polarity reverses, and direction of current is opposite through *R* for positive and negative half cycles so out put is not rectified.

Since R_1 and R_2 are different hence the peaks during positive half and negative half of the input signal will be different.

17. (b) In half wave rectifier $V_{dc}=\frac{V_0}{\pi}=\frac{10}{\pi}$

18. (a) In common base mode α = 0.98, R_L = 5 $k\Omega$, R_{in}= 70Ω

$$\therefore\ \text{voltage gain } A_v=\alpha\times\frac{R}{R_{in}}=0.98\times\frac{5\times10^3}{70}=70$$

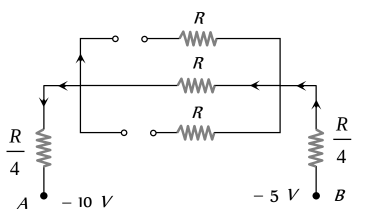
Power gain = Current gain $\times$ Voltage gain

= 0.98 $\times$ 70 = 68.6

19. (a) $r_n=\varepsilon_r\left(\frac{n^2}{Z}\right)a_o=12\times\frac{(5^2)}{15}\times0.53$ = 10.6 Å.

20. (c) (i) V_A = –10 *V* and V_B = –5 *V*

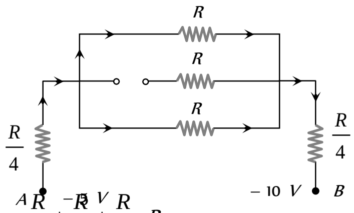
Diodes D_1 and D_3 are reveres biased and D_2 is forward biased.



$$\Rightarrow R_{AB} = R + \frac{R}{4} + \frac{R}{4} = \frac{3}{2}R.$$

(ii) When $V_A = -5\,V$ and $V_B = -10\,V$

Diodes D_1 is reverse biased D_2 and D_3 are forward biased



$$\Rightarrow R_{AB} = \frac{R}{4} + \frac{R}{2} + \frac{R}{4} = R.$$

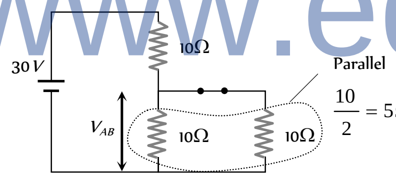
(iii) In this case equivalent resistance between A and B is also R.

Hence (ii) = (iii) < (i).

21. (b) According to the given polarity, diode D_1 is forward biased while D_2 is reverse biased. Hence current will pass through D_1 only.

So current $i = \dfrac{6}{(150+50+100)} = 0.02\,A$

22. (a) Diode is in forwards biasing hence the circuit can be redrawn as follows



$$V_{AB} = \frac{30}{(10+5)} \times 5 = 10\,V$$

23. (d) The diode D will conduct for positive half cycle of *a.c.* supply because this is forward biased. For negative half cycle of *a.c.* supply, this is reverse biased and does not conduct. So out put would be half wave rectified and for half wave rectified out put

$$V_{rms} = \frac{V_0}{2} = \frac{200\sqrt{2}}{2} = \frac{200}{\sqrt{2}}$$

24. (d) $\sigma = ne(\mu_e + \mu_h) = 2\times10^{19} \times 1.6\times10^{-19}(0.36+0.14)$

$= 1.6\,(\Omega\text{-}m)^{-1}$

$$R = \rho\frac{l}{A} = \frac{l}{\sigma A} = \frac{0.5\times10^{-3}}{1.6\times10^{-4}} = \frac{25}{8}\,\Omega$$

$$\therefore\ i = \frac{V}{R} = \frac{2}{25/8} = \frac{16}{25}A = 0.64\,A$$

25. (a) As we know current density $J = nqv$

$\Rightarrow J_e = n_e q v_e$ and $J_h = n_h q v_h$

$$\Rightarrow \frac{J_e}{J_h} = \frac{n_e}{n_h}\times\frac{v_e}{v_h} \Rightarrow \frac{3/4}{1/4} = \frac{n_e}{n_h}\times\frac{5}{20} \Rightarrow \frac{n_e}{n_h} = \frac{6}{5}$$

26. (b) Consider the case when Ge and Si diodes are connected as show in the given figure.

Equivalent voltage drop across the combination Ge and Si diode = 0.3 V

$\Rightarrow$ Current $i = \dfrac{12-0.3}{5\,k\Omega} = 2.34\,mA$

$\therefore$ Out put voltage $V_0 = Ri = 5\,k\Omega \times 2.34\,mA = 11.7\,V$

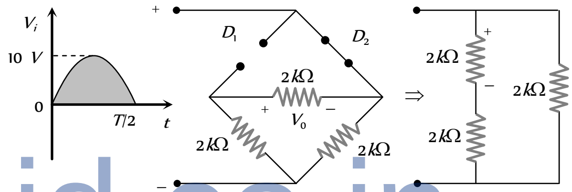
Now consider the case when diode connection are reversed. In this case voltage drop across the diode's combination = 0.7 V

$\Rightarrow$ Current $i = \dfrac{12-0.7}{5\,k\Omega} = 2.26\,mA$

$\therefore\ V_0 = iR = 2.26\,mA \times 5\,k\Omega = 11.3\,V$

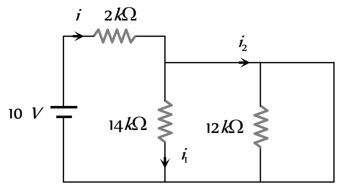
Hence charge in the value of V_0 = 11.7 – 11.3 = 0.4 V

27. (b) For the positive half cycle of input the resulting network is shown below



$$\Rightarrow (V_0)_{max} = \frac{1}{2}(V_i)_{max} = \frac{1}{2}\times10 = 5\,V.$$

28. (d) The equivalent circuit can be redrawn as follows



From figure it is clear that current drawn from the battery

$i = i_2 = \dfrac{10}{2} = 5mA$ and $i_1 = 0$.

29. (c) $i_b = \dfrac{5-0.7}{8.6} = 0.5\,mA \Rightarrow I_c = \beta I_b = 100\times0.5\,mA$

By using $V_{CE} = V_{CC} - I_c R_L = 18 - 50\times10^{-3}\times100 = 13V$

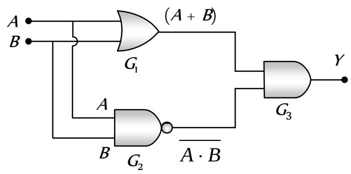
30. (a) $I_e = 10^{10}\times1.6\times10^{-19}\times\dfrac{1}{10^{-6}} = 1.6\,mA$ $\left(\because I = \dfrac{Q}{t}\right)$

Since 2% electrons are absorbed by base, hence 98% electrons reaches the collector *i.e.* α = 0.98

$\Rightarrow I_c = \alpha I_e = 0.98\times1.6 = 1.568\,mA \approx 1.57\,mA$

Also current amplification factor $\beta = \dfrac{\alpha}{1-\alpha} = \dfrac{0.98}{0.02} = 49$

31. (b)



$Y = (A+B).\overline{AB}$

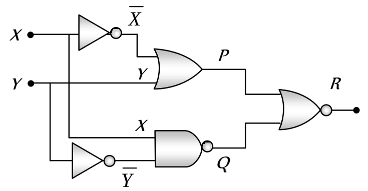
The given output equation can also be written as

$Y = (A+B).(\overline{A}+\overline{B})$ (De morgan's theorem)

$= A\overline{A} + A\overline{B} + B\overline{A} + B\overline{B} = 0 + A\overline{B} + \overline{A}B + 0 = \overline{A}B + A\overline{B}$

This is the expression for XOR gate.

32. (c)

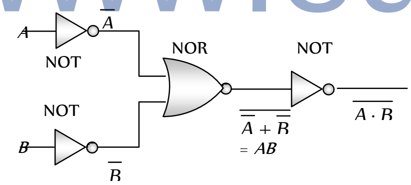


The truth table can be written as

X	Y	$\overline{X}$	$\overline{Y}$	$P = \overline{X} + Y$	$Q = \overline{X.\overline{Y}}$	$R = \overline{P + Q}$
0	1	1	0	1	1	0
1	1	0	0	1	1	0
1	0	0	1	0	0	1
0	0	1	1	1	1	0

Hence $X = 1$, $Y = 0$ gives output $R = 1$

33. (d)



Hence option (d) is correct.

34. (b) The truth table of the circuit is given

A	B	C	$X = \overline{AB}$	$Y = \overline{BC}$	$Z = \overline{X+Y}$
0	0	0	1	1	0
1	0	0	1	1	0
0	0	1	1	1	0
1	0	1	1	1	0
0	1	0	1	1	0
1	1	0	0	1	0
0	1	1	1	0	0
1	1	1	0	0	1

Output Z of single three input gate is that of AND gate.

35. (c) Output of upper OR gate = $W + X$

Output of lower OR gate = $W + Y$

Net output $F = (W + X)(W + Y)$

$= WW + WY + XW + XY$ (Since $WW = W$)

$= W(1 + Y) + XW + XY$ (Since $1 + Y = 1$)

$= W + XW + XY = W(1 + X) + XY = W + XY$

36. (b) $\mu = r_p\, g_m = 50$

From $i_p = KV_p^{3/2} \Rightarrow \frac{\Delta V_p}{\Delta i_p} = r_p = \frac{2 i_p^{-1/3}}{3K^{2/3}}$

$\Rightarrow g_m = \frac{\mu}{r_p} = \frac{3\mu K^{2/3} i_p^{1/3}}{2} = \frac{3}{2}\mu K^{2/3}\left[K^{1/3}(V_p + \mu V_g)^{1/2}\right]$

$= \frac{3}{2}\mu K(V_p + \mu V_g)^{1/2} = 75\ K\,(i_p/K)^{1/3}$

Because i_p was in mA, g_m is substituted as 5 $m℧$

$\Rightarrow 5 = 75K^{2/3} i_p^{1/3} = 75\,K^{2/3}(8)^{1/3} \Rightarrow K = \left(\frac{1}{30}\right)^{3/2}$

Cut off grid voltage $V_G = -\frac{V_p}{\mu} = -\frac{300}{50} = -6V$

37. (d) $g_m = \left(\frac{\Delta i_p}{\Delta V_g}\right)_{V_p = \text{constant}} = \frac{(15-10)\times 10^{-3}}{0-(-4)} = 1.25 \times 10^{-3}\Omega$

$\mu = \left(\frac{\Delta V_p}{\Delta V_g}\right)_{I_p = \text{constant}} = \frac{150-120}{0-(-4)} = 7.5$

$\therefore r_p = \frac{\mu}{g_m} = \frac{7.5}{1.25 \times 10^{-3}} = 6000\ ohms$

38. (d) The dynamic plate resistance is $r_p = \frac{\Delta V_p}{\Delta i_p}$

Now for a vacuum diode $i_p = KV_p^{3/2} \Rightarrow V_p = \left(\frac{i_p}{K}\right)^{2/3}$

$\Rightarrow \frac{\Delta V_p}{\Delta i_p} = \frac{2}{3\,K^{2/3}} i_p^{\left(\frac{2}{3}-1\right)}$

$\Rightarrow r_p = (\text{constant}) I_p^{-1/3} \Rightarrow r_p \propto \frac{1}{I_p^{1/3}}$

39. (d) $i_p = [0.125\,V_p - 7.5] \times 10^{-3}\ amp$

Differentiating this equation $w.r.t.\ V_p$

$\frac{\Delta i_p}{\Delta V_p} = 0.125 \times 10^{-3}$ or $\frac{1}{r_p} = 0.125 \times 10^{-3} \Rightarrow r_p = 8\,k\Omega$

40. (b) $V_{peak} = \sqrt{2}\ \ V_{rms} = \sqrt{2} \times 141.4 = 200\ V$

41. (c) The emission current $i = AT^2 S e^{-\phi/kT}$

For the two surfaces $A_1 = A_2$, $S_1 = S_2$, $T_1 = 800\ K$, $T_2 = 1600\,K, \phi_1 / T_1 = \phi_2 / T_2$

Therefore, $\frac{i_2}{i_1} = \left(\frac{T_2}{T_1}\right)^2 = (2)^2 = 4 \Rightarrow i_2 = 4i_1 = 4\,mA.$

42. (a) The first data gives value of plate resistance $r_p = \frac{\Delta V_p}{\Delta i_p} = \frac{10}{0.8 \times 10^{-3}} = \frac{10^5}{8}\Omega$

Also $g_m = \frac{\Delta i_p}{\Delta V_g}$ and $g_m = \frac{\mu}{r_p}$

$$\Rightarrow \Delta V_g = \frac{\Delta i_p \times r_p}{\mu} = \frac{4\times10^{-3}\times10^5/8}{8} = 6.25\ V$$

43. (a) $I_p = 0.004\,(V_p + 10V_g)^{3/2}$

$$\Rightarrow \frac{\Delta I_p}{\Delta V_g} = 0.004\left[\frac{3}{2}(V_p+10V_g)^{1/2}\times10\right]$$

$$\Rightarrow g_m = 0.004\times\frac{3}{2}(120+10\times-2)^{1/2}\times10$$

$$\Rightarrow g_m = 6\times10^{-4}\,mho = 0.6\,m\,mho$$

Comparing the given equation of I_p with standard equation $I_p = K(V_p+\mu V_g)^{3/2}$ we get $\mu = 10$

Also from $\mu = r_p \times g_m \Rightarrow r_p = \frac{\mu}{g_m} = \frac{10}{0.6\times10^{-3}}$

$$\Rightarrow r_p = 16.67\times10^3\Omega = 16.67\,k\Omega.$$

44. (b) $\mu = r_p \times g_m = 20\times2.5 = 50$

From $A = \frac{\mu R_L}{r_p+R_L} \Rightarrow r_p + R_L = \frac{\mu R_L}{A} = \frac{50R_L}{10} = 5R_L$

$$\Rightarrow 4R_L = r_p \Rightarrow R_L = \frac{r_p}{4} = \frac{20}{4} = 5k\Omega$$

45. (a) $A = \frac{\mu R_L}{r_p+R_L} = \frac{14\times12}{10+12} = \frac{84}{11}$. Peak value of output signal

$$V_0 = \frac{84}{11}\times2\sqrt{2}V \Rightarrow V_{rms} = \frac{V_0}{\sqrt{2}} = \frac{84\times2}{11}V$$

$\Rightarrow$ *r.m.s.* value of current through the load

$$= \frac{84\times2}{11\times12\times10^3}A = 1.27\,mA$$

46. (c) $r_p = \frac{\mu}{g_m} = \frac{64}{1600\times10^{-6}} = 4\times10^4\Omega$

Voltage gain $A_v = \frac{\mu}{1+\frac{r_p}{R_L}} = \frac{64}{1+\frac{4\times10^4}{40\times10^3}} = 32$

$\therefore$ Output signal voltage

$$V_0 = A_v\times V_i = 32\times1 = 32\,V(r.m.s.)$$

Signal power in load $= \frac{V_0^2}{R_L} = \frac{(32)^2}{40\times10^3} = 25.6\,mW$

47. (a) $i_p = k(V_p+\mu V_g)^{3/2}mA$

$\Rightarrow 4 = k(200-10\times4)^{3/2} = k\times(160)^{3/2}$ ....(i)

and $i_p = k(160-10\times7)^{3/2} = k\times(90)^{3/2}$ ....(ii)

From equation (i) and (ii) we get

$$i_p = 4\times\left(\frac{90}{160}\right)^{3/2} = 4\times\left(\frac{3}{4}\right)^3 = 1.69\,mA$$

48. (a) At $V_g = -3V, V_p = 300\ V$ and $I_p = 5mA$

At $V_g = -1V$, for constant plate current *i.e.* $I_p = 5mA$

From $I_p = 0.125\,V_p - 7.5$

$$\Rightarrow 5 = 0.125V_p - 7.5 \Rightarrow V_p = 100V$$

$\therefore$ change in plate voltage $\Delta V_p = 300-100 = 200V$

Change in grid voltage $\Delta V_g = -1-(-3) = 2V$

So, $\mu = \frac{\Delta V_p}{\Delta V_g} = \frac{200}{2} = 100$

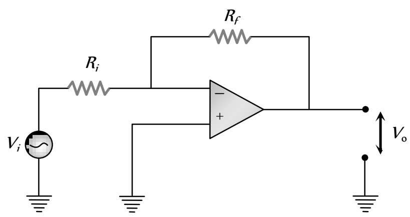
49. (b) The slope of anode characteristic curve $= \frac{1}{r_p}$

$$\Rightarrow r_p = \frac{1}{0.02\,mA/V} = 50\frac{V}{mA} = 50\times10^3\frac{V}{A}$$

The slope of mutual characteristic curve $= g_m = 1\times10^{-3}\ A/V$.

$$\therefore \mu = r_p\times g_m = 50\times10^3\times10^{-3} = 50.$$

50. (b) Voltage gain $A = \frac{V_o}{V_i} = \frac{R_f}{R_i} = \frac{100\,k\Omega}{1\,k\Omega} = 100$.



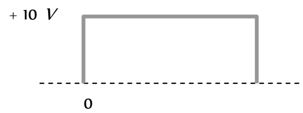
Graphical Questions

1. (c) With rise in temperature, resistivity of semiconductors decreases exponentially.

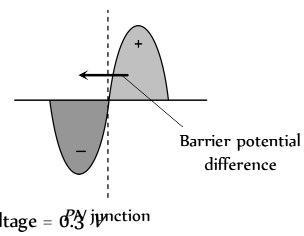
2. (b) Potential across the *PN* junction varies symmetrically linear, having *P* side negative and *N* side positive.

3. (c) *PN* junction has low resistance in one direction of potential difference $+V$, so a large current flows (forward biasing). It has a high resistance in the opposite potential difference direction $-V$, so a very small current flows (Reverse biasing).

4. (c) When input voltage is $-10\ V$, the diode is reverse biased and no output is obtained. On the other hand, when input is $+10\ V$, the diode is forward biased and output is obtained which is $+10\ V$. Therefore the output is of the form as show in the following figure.



5. (a) In the depletion layer of *PN* junction, stationary, positive ions exists in the *N*-side and stationary negative ions exists in the *P* side.



6. (b) V_k = knee voltage = 0.3 V

$$\therefore \text{Resistance} = \frac{\Delta V}{\Delta i} = \frac{(2.3-0.3)}{(10-0)\times10^{-3}} = 200\Omega = 0.2k\Omega$$

7. (b) Half wave rectifier, rectifies only the half cycle of input ac signal and it blocks the other half.

8. (c) As RC time constant of the capacitor is quite large ($\tau = RC = 10 \times 10^3 \times 10 \times 10^{-6} = 0.1\, sec$), if will not discharge appreciably. Hence voltage remains nearly constant.

9. (b) In the positive half cycle of input ac signal diode D_1 is forward biased and D_2 is reverse biased so in the output voltage signal, A and C are due to D_1. In negative half cycle of Input ac signal D_2 conducts, hence output signals B and D are due to D_2.

10. (a) If i is the current in the diode and V is voltage drop across it, then for given figure voltage equation is

$$i \times 100 + V = 8 \Rightarrow i = -\frac{1}{100}V + \frac{8}{100} \Rightarrow i = -(0.01)V + 0.08$$

Thus the slope of i-V graph $= \frac{1}{R_L} = 0.01$

11. (b) The current at 2 V is 400 mA and at 2.1 V it is 800 mA. The dynamic resistance in this region

$$R = \frac{\Delta V}{\Delta i} = \frac{(2.1 - 2)}{(800 - 400) \times 10^{-3}} = \frac{1}{4} = 0.25\Omega$$

12. (a) From the given waveforms, the following truth table can be made

Time interval	Inputs		Output
	A	B	Y
$0 \to T_1$	0	0	0
$T_1 \to T_2$	0	1	0
$T_2 \to T_3$	1	0	0
$T_3 \to T_4$	1	1	1

This truth table is equivalent to 'AND' gate.

13. (d) 5 *volt* is low signal (0) and 10 *volt* is high signal (1) and taking 5 μ-*sec* as 1 unit. In a negative logic, low signal (0) gives high output (1) and high signal (1) gives low output (0). The output is therefore 1010010111.

14. (a) $g_m = \frac{\Delta i_p}{\Delta V_g} = \frac{(20 - 15) \times 10^{-3}}{(4 - 2)} = 2.5\, millimho$

15. (d) The cut off grid voltage is that negative grid bias corresponding to which the plate current becomes zero. At point P, $i_p = 0$

16. (a) According to Richardson-Dushman equation $J = AT^2 e^{-b/T}$

Taking log of this equation $\log_e \frac{J}{T^2} = \log_e A - \frac{b}{T}$

i.e. graph between $\log_e \frac{J}{T^2}$ and $\frac{1}{T}$ will be a straight line having negative slope and positive intercept ($\log_e A$) on $\log_e \frac{J}{T^2}$ axis.

17. (c) $J = AT^2 e^{-b/T} \Rightarrow \frac{J}{T^2} \propto e^{-b/T}$

i.e. $\frac{J}{T^2}$ will vary exponentially with $\frac{1}{T}$, having negative slope.

18. (c) This is the graph between i_p and V_g and i_p becomes zero at certain negative potential.

19. (a) $\mu = -\left(\frac{\Delta V_p}{\Delta V_g}\right)_{\Delta i_p = \text{const.}} = \frac{-(80 - 60)}{[-6 - (-4)]} = \frac{20}{2} = 10$

20. (c) According to $|A_v| = \frac{\mu}{1 + \frac{r_p}{R_L}}$

as R_L increases A_v also increases. When R_L becomes too high then A_v = maximum = μ

Hence only option (c) is correct.

21. (c) With rise in temperature, work function decreases (non-linearly).

22. (c) $R_p = \frac{V_p}{i_p} = \frac{50}{150 \times 10^{-3}} = 333.3\,\Omega$

23. (a) $i \propto T^2 \Rightarrow \frac{i}{i_0} = \left(\frac{T}{T_0}\right)^2$

This is the equation of a parabola.

24. (b) The band width is defined as the frequency band in which the amplifier gain remains above $\frac{1}{\sqrt{2}} = 0.707$ of the mid frequency gain (A_{max}). The low frequency f_1 at which the gain falls to $\frac{1}{\sqrt{2}}$ *i.e.* 0-.707 times it's mid frequency value is called lower cut off frequency and the high frequency f_4 at which the gain falls to $\frac{1}{\sqrt{2}}$ *i.e.* 0.707 times of it's mid frequency is known as higher cut off frequency so band width = $f_4 - f_1$.

25. (c) r_p varies with i_p according to relation $r_p \propto i_p^{-1/3}$ *i.e.* when i_p increases, r_p decreases, hence graph C represents the variation of r_p.

μ doesn't depends upon i_p, hence graph A is correct.

26. (c) From the graph it is clear that of for $V_g = -4V, i_p = 0$, so cut off voltage is – 4 *volt*.

27. (b) As temperature increases saturation current also increases.

28. (c)

29. (a) Output signal voltage has phase difference of 180° with respect to input.

30. (d) Grid is maintained between 0 *volt* to certain negative voltage.

Assertion and Reason

1. (d) In diode the output is in same phase with the input therefore it cannot be used to built NOT gate.

2. (a) According to law of mass action, $n_i^2 = n_e n_h$. In intrinsic semiconductors $n_i = n_e = n_h$ and for P-type semiconductor n_e would be less than n_i, since n_h is necessarily more than n_i.

3. (c) In common emitter transistor amplifier current gain $\beta > 1$, so output current > Input current, hence assertion is correct.

Also, input circuit has low resistance due to forward biasing to emitter base junction, hence reason is false.

4. (a) Input impedance of common emitter configuration

$$= \left.\frac{\Delta V_{BE}}{\Delta i_B}\right|_{V_{CE} = \text{constant}}$$

where ΔV_{BE} = voltage across base and emitter (base emitter region is forward biased)

Δi_B = base current which is order of few microampere.

Thus input impedance of common emitter is low.

5. (d) Resistivity of semiconductors decreases with temperature. The atoms of a semiconductor vibrate with larger amplitudes at higher temperatures there by increasing it's conductivity not resistivity.

6. (a) In semiconductors the energy gap between conduction band and valence band is small ($\approx$ 1 *eV*). Due to temperature rise, electron in the valence band gained thermal energy and may jump across the small energy gap, goes in to the conduction band. Thus conductivity increases and hence resistance decreases.

7. (b)

8. (a) The ratio of the velocity to the applied field is called the mobility. Since electron is lighter than holes, they move faster in applied field than holes.

9. (b) Intrinsic semiconductor (Neutral) + Pentalvalent impurity (Neutral) → *N*-type semiconductor (Neutral)

10. (a) At a particular temperature all the bonds of crystalline solids breaks and show sharp melting point.

11. (c) The energy gap for germanium is less $(0.72 eV)$ than the energy gap of silicon $(1.1 eV)$. Therefore, silicon is preferred over germanium for making semiconductor devices.

12. (e) We cannot measure the potential barrier of a *PN*-junction by connecting a sensitive voltmeter across its terminals because in the depletion region, there are no free electrons and holes and in the absence of forward biasing, *PN*- junction offers infinite resistance.

13. (e) The assertion is not true. In fact, semiconductor Obeys Ohm's law for low values of electric field (~ 10· *V/m*). Above this, the current becomes almost independent of electric field.

14. (d) Two *PN*-junctions placed back to back cannot work as *NPN* transistor because in transistor the width and concentration of doping of *P*-semiconductor is less as compared to width doping of *N*-type semiconductor type.

15. (b) Common emitter is prepared over common base because all the current, voltage and power gain of common emitter amplifier is much more than the gains of common base amplifier.

16. (d) In *PN*-junction, the diffusion of majority carriers takes place when junction is forward biased and drifting of minority carriers takes place across the function, when reverse biased. The reverse bias opposes the majority carriers but makes the minority carriers to cross the *PN*-junction. Thus the small current in μA flows during reverse bias.

17. (d) A transistor is a current operating device because the action of transistor is controlled by the charge carriers (electrons or holes). Base current is very much lesser than the collector current.

18. (a) These gates are called digital building blocks because using these gates only (either NAND or NOR) we can compile all other gates also (like OR, AND, NOT, XOR).

19. (d) At 0*K*, Germanium offers infinite resistance, and it behaves as an insulator.

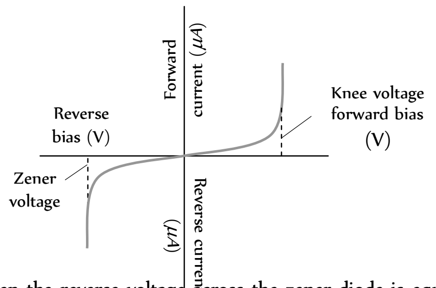
20. (a) In a transistor, the base is made extremely thin to reduce the combinations of holes and electrons. Under this condition, most of the holes (or electrons) arriving from the emitter diffuses across the base and reach the collector. Hence, the collector current, is almost equal to the emitter current, the base current being comparatively much smaller. This is the main reason that power gain and voltage gain are obtained by a transistor. If the base region was made quite thick, then majority of carriers from emitter will combine with the carriers in the base and only small number of carriers will reach the collector, so there would be little collector current and the purpose of transistor would be defeated.

21. (c) The current gain in common base circuit $\alpha = \left(\frac{\Delta I_C}{\Delta I_E}\right)_{V_C}$

The change in collector current is always less than the change in emitter current.

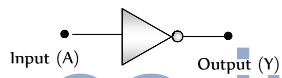
$\Delta I_C < \Delta I_E$. Therefore, $\alpha < 1$.

22. (d) The *V-i* characteristic of *PN*- diode depends whether the junction is forward biased or reverse biased. This can be showed by graph between voltage and current.



23. (a) When the reverse voltage across the zener diode is equal to or more than the breakdown voltage, the reverse current increases sharply.

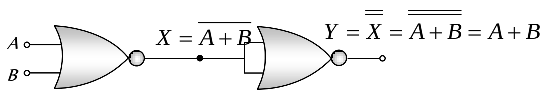
24. (a)



If *A* = 0, *Y* = 1 and *A* = 1, *Y* = 0.

25. (b) In vacuum tubes, vacuum is necessary and the working of semiconductor devices is independent of heating or vacuum.

26. (a)



This is the Boolean expression for 'OR' gate.

27. (a) For detection of a particular wavelength (λ) by a *PN* photo diode, energy of incident light > E_g $\Rightarrow \frac{hc}{E_g} > \lambda$

For $E_g = 2.8\, eV, \frac{hc}{E_g} = \frac{6.6 \times 10^{-34} \times 3 \times 10^{8}}{2.8 \times 1.6 \times 10^{-19}} = 441.9\, nm$

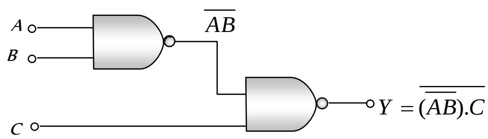
i.e. $\frac{hc}{E_g} < 6000\, nm$, so diode will not detect the wavelength of 6000Å.

28. (a)

29. (b) In forward biasing of *PN* junction current flows due to diffusion of majority charge carriers. While in reverse biasing current flows due to drifting of minority charge carriers.

The circuit given in the reason is a *PNP* transistor having emitter is more negative *w.r.t.* base so it is reverse biased and collector is more positive *w.r.t.* base so it is forward biased.

30. (c) Assertion is true but reason is false



If $A = 1$, $B = 0$, $C = 1$ then $Y = 0$

31. (b) Both assertion and reason are true but potential difference across the resistance is zero, because diode is in reverse biasing hence no current flows.

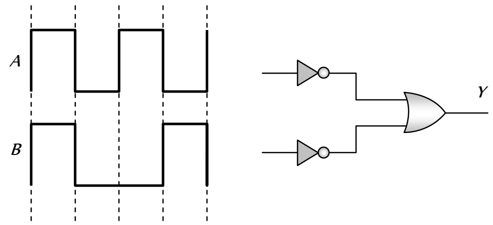
Electronics

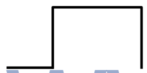
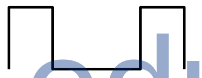
SET Self Evaluation Test - 27

1. In a pure silicon ($n_i = 10^{16}/m^3$) crystal at 300 K, 10^{21} atoms of phosphorus are added per cubic meter. The new hole concentration will be
   (a) 10^{21} per m^3 (b) 10^{19} per m^3
   (c) 10^{11} per m^3 (d) 10^{5} per m^3

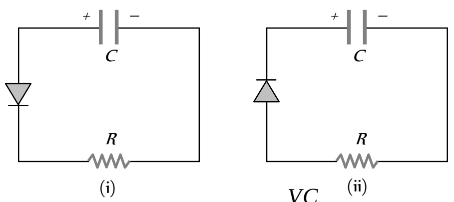
2. In the Boolean algebra $(\overline{\overline{A}\cdot\overline{B}})\cdot A$ equals to
   (a) $\overline{A+B}$ (b) A
   (c) $\overline{A\cdot B}$ (d) $A+B$

3. In a given circuit as shown the two input waveform A and B are applied simultaneously. The resultant waveform Y is



   (a)  (b) 
   (c)  (d) 

4. Two identical capacitors A and B are charged to the same potential V and are connected in two circuits at $t = 0$, as shown in figure. The charge on the capacitors at time $t = CR$ are respectively

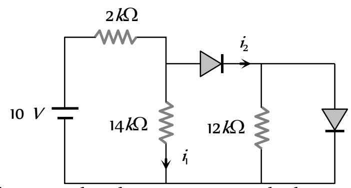


   (a) VC, VC (b) $\frac{VC}{e}$, VC
   (c) VC, $\frac{VC}{e}$ (d) $\frac{VC}{e}$, $\frac{VC}{e}$

5. In transistor, forward bias is always smaller than the reverse bias. The correct reason is
   (a) To avoid excessive heating of transistor
   (b) To maintain a constant base current
   (c) To produce large voltage gain
   (d) None of these

6. In NPN transistor, if doping in base region is increased then collector current
   (a) Increases (b) Decreases
   (c) Remain same (d) None of these

7. In the following circuit I_1 and I_2 are respectively



   (a) 0, 0
   (b) 5 mA, 5 mA
   (c) 5 mA, 0
   (d) 0, 5 mA

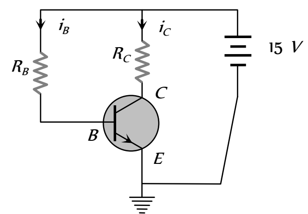
8. In space charge limited region, the plate current in a diode is 10 mA for plate voltage 150 V. If the plate voltage is increased to 600 V, then the plate current will be
   (a) 10 mA (b) 40 mA
   (c) 80 mA (d) 160 mA

9. A triode has a plate resistance of 10 $k\Omega$ and amplification factor 24. If the input signal voltage is 0.4 V ($r.m.s.$), and the load resistance is 10 k ohm, then, the output voltage ($r.m.s.$) is
   (a) 4.8 V (b) 9.6 V
   (c) 12.0 V (d) None of these

10. Pure sodium (Na) is a good conductor of electricity because the $3s$ and $3p$ atomic bands overlap to form a partially filled conduction band. By contrast the ionic sodium chloride ($NaCl$) crystal is
   (a) Insulator (b) Conductor
   (c) Semiconductor (d) None of these

11. Would there be any advantage to adding n-type or p-type impurities to copper
   (a) Yes (b) No
   (c) May be (d) Information is insufficient

12. In the following common emitter circuit if $\beta = 100$, $V_{CE} = 7V$, V_{BE} = Negligible $R_C = 2\ k\Omega$ then I_B = ?

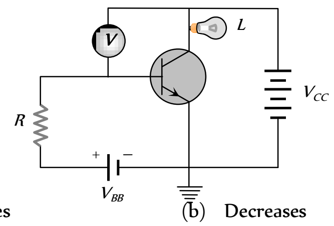


   (a) 0.01 mA
   (b) 0.04 mA
   (c) 0.02 mA
   (d) 0.03 mA

13. When a battery is connected to a P-type semiconductor with a metallic wire, the current in the semiconductor (predominantly), inside the metallic wire and that inside the battery respectively due to
   (a) Holes, electrons, ions (b) Holes, ions, electrons
   (c) Electrons, ions, holes (d) Ions, electrons, holes

14. Is the ionisation energy of an isolated free atom different from the ionisation energy E_g for the atoms in a crystalline lattice
   (a) Yes (b) No
   (c) May be (d) None of these

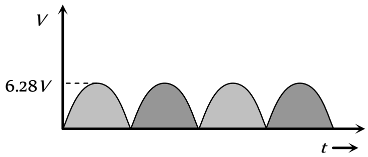
15. In the following circuit, a voltmeter V is connected across a lamp L. What change would occur in voltmeter reading if the resistance R is reduced in value



(a) Increases (b) Decreases

(c) Remains same (d) None of these

16. For given electric voltage signal dc value is



(a) 6.28 V (b) 3.14 V

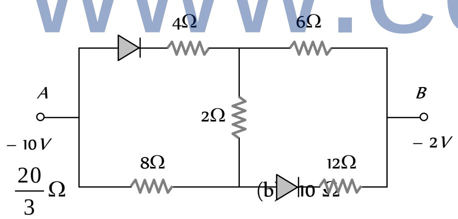
(c) 4 V (d) 0 V

17. When a silicon PN junction is in forward biased condition with series resistance, it has knee voltage of 0.6 V. Current flow in it is 5 mA, when PN junction is connected with 2.6 V battery, the value of series resistance is

(a) 100 Ω (b) 200 Ω

(c) 400 Ω (d) 500 Ω

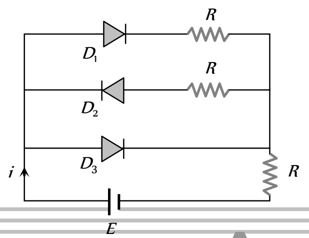
18. In the following circuit the equivalent resistance between A and B is



(a) $\frac{20}{3}\,\Omega$ (b) 10 Ω

(c) 16 Ω (d) 20 Ω

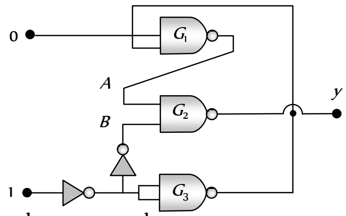
19. In the following circuit of PN junction diodes D_1, D_2 and D_3 are ideal then i is



(a) E/R (b) $E/2R$

(c) $2E/3R$ (d) Zero

20. In circuit in following fig. the value of Y is



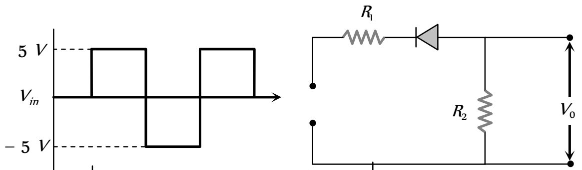
(a) 0

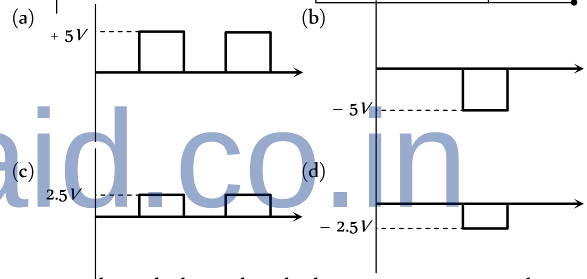
(b) 1

(c) Fluctuates between 0 and 1

(d) Indeterminate as the circuit can't be realised

21. A waveform shown when applied to the following circuit will produce which of the following output waveform. Assuming ideal diode configuration and $R_1 = R_2$





22. In a triode, cathode, grid and plate are at 0, – 2 and 80 V respectively. The electrons is emitted from the cathode with energy 3 eV. The energy of the electron reaching the plate is

(a) 77 eV (b) 85 eV

(c) 81 eV (d) 83 eV

23. The energy gap of silicon is 1.5 eV. At what wavelength the silicon will stop to absorb the photon

(a) 8250 Å (b) 7250 Å

(c) 6875.5 Å (d) 5000 Å

AS Answers and Solutions

(SET -27)

1. (c) By using mass action law $n_i^2 = n_e n_h$

$$\Rightarrow n_h = \frac{n_i^2}{n_e} = \frac{(10^{16})^2}{10^{21}} = 10^{11}\ per\ m^3$$

2. (b) $(\overline{\overline{A}\cdot\overline{B}})\cdot A = (\overline{\overline{A+B}})\cdot A = (A+B)\cdot A$

$= A \cdot A + AB = A + AB = A(1 + B) = A$

3. (a) (1 = high, 0 = low)

Input to A is in the sequence, 1,0,1,0.

Input to B is in the sequence, 1, 0, 0, 1.

Sequence is inverted by NOT gate.

Thus inputs to OR gate becomes 0, 1, 0, 1 and output of OR gate becomes 0, 1, 1, 1

Since for OR gate 0 + 1 = 1. Hence choice (a) is correct.

4. (b) Time $t = CR$ is known as time constant. It is time in which charge on the capacitor decreases to $\frac{1}{e}$ times of it's initial charge (steady state charge).

In figure (i) PN junction diode is in forward bias, so current will flow the circuit *i.e.*, charge on the capacitor decrease and in time t it becomes $Q = \frac{1}{e}(Q_o)$; where $Q_o = CV$

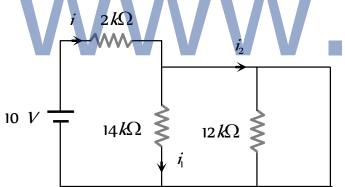
$\Rightarrow Q = \frac{CV}{e}$

In figure (ii) P-N junction diode is in reverse bias, so no current will flow through the circuit hence change on capacitor will not decay and it remains same *i.e.* CV after time t.

5. (a) If forward bias is made large, the majority charge carriers would move from the emitter to the collector through the base with high velocity. This would give rise to excessive heat causing damage to transistor.

6. (b) Number of holes in base region increases hence recombination of electron and hole are also increases in this region. As result base current increases which in turn decreases the collector current.

7. (d) Equivalent circuit can be redrawn as follows



$i = \frac{10}{2} = 5\,mA = i_2$

$i_1 = 0$

8. (c) In space charge limited region, the plate current is given by Child's law $i_p = KV_p^{3/2}$

Thus, $\frac{i_{p_2}}{i_{p_1}} = \left(\frac{V_{p_2}}{V_{p_1}}\right)^{3/2} = \left(\frac{600}{150}\right)^{3/2} = (4)^{3/2} = 8$

or $i_{p_2} = i_{p_1} \times 8 = 10 \times 8\ mA = 80\ mA$.

9. (a) Use $V_0 = AV_s$

Now $A = \frac{24 \times 10k}{10k + 10k} = \frac{24 \times 10}{20} = 12$

Therefore, $V_0 = 12 \times 0.4 = 4.8\,volt(r.m.s.)$

10. (a) In sodium chloride the Na^+ and Cl^- ions both have noble gas electron configuration corresponding to completely filled bands. Since the bands do not overlap, there must be a gap between the filled bands and the empty bands above them, so $NaCl$ is an insulator.

11. (b) Pure Cu is already an excellent conductor, since it has a partially filled conduction band, furthermore, Cu forms a metallic crystal as opposed to the covalent crystals of silicon or germanium, so the scheme of using an impurity to donate or accept an electron does not work for copper. In fact adding impurities to copper decreases the conductivity because an impurity tends to scatter electrons, impeding the flow of current.

12. (b) $V = V_{CE} + I_C R_L$

$\Rightarrow 15 = 7 + I_c \times 2 \times 10^3 \Rightarrow i_c = 4\ mA$

$\because \beta = \frac{i_C}{i_B} \Rightarrow i_B = \frac{4}{100} = 0.04\,mA$

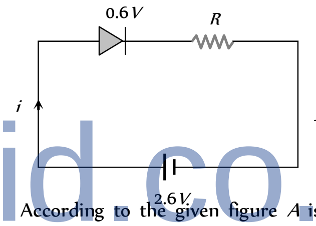
13. (a) Charge carriers inside the P-type semiconductor are holes (mainly). Inside the conductor charge carriers are electrons and for cell ions are the charge carriers.

14. (a) The ionisation energy of an isolated atom is different from it's value in crystalline lattice, because in the latter case each bound electron is influenced by many atoms in the periodic crystalline lattice.

15. (a) Here the emitter base junction of N-P-N transistor is forward biased with battery V_{BB} through resistance R. When the value of R is reduced, then the emitter current i_e will increase. As a result the collector current will also increase. ($i_c = i_e - i_b$). Due to increase in i_c, the potential difference across R_L increases and hence the reading of voltmeter will increases.

16. (c) $V_{dc} = V_{ac} = \frac{2V_0}{\pi} = \frac{2 \times 6.28}{3.14} = 4V.$

17. (c)

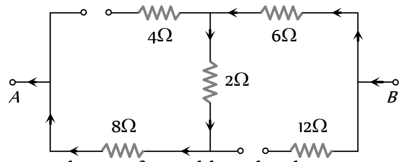


$R = \frac{(2.6 - 0.6)}{5 \times 10^{-3}} = 400\ \Omega.$

18. (c) According to the given figure A is at lower potential *w.r.t.* B. Hence both diodes are in reverse biasing, so equivalent, circuit can be redrawn as follows.

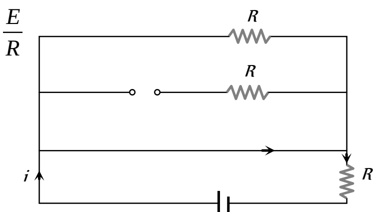
$\Rightarrow$ Equivalent resistance between A and B

$R = 8 + 2 + 6 = 16\ \Omega.$



19. (a) Diodes D_1 and D_3 are forward biased and D_2 is reverse biased so the circuit can be redrawn as follows.

$\Rightarrow i = \frac{E}{R}$



20. (a) Lower NOT gate inverts input 1 to zero. NOT gate from NAND gate inverts this output to 1 upper NAND gate converts this input 1 and input 0 to 1.

Thus $A = 1$ and $B = 1$ become inputs of NAND gate giving final output as zero. Choice A is correct.

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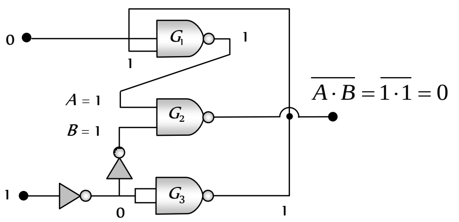
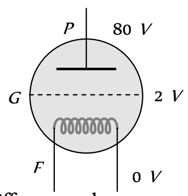


21. (d) The *P-N* junction will conduct only when it is forward biased *i.e.* when – 5*V* is fed to it, so it will conduct only for 3rd quarter part of signal shown and when it conducts potential drop 5 *volt* will be across both the resistors, so output voltage across R_L is 2.5 *V*.

$\therefore \ V_0 = -2.5\,V$

22. (d) There is a loss of kinetic energy of 2 *eV* from filament to grid. The energy of the electron after passing through the grid will be 3 – 2 = 1 *eV*



The potential difference between plate and grid is $80-(-2)=82V$. The electron will gain energy 82 *eV* from the grid to the plate. The energy of electron reaching the plate = 1 + 82 = 83 *eV*

23. (a) $\lambda = \frac{hc}{E} = \frac{6.6\times10^{-34}\times3\times10^{8}}{1.5\times1.6\times10^{-19}} = 8.25\times10^{-7}m = 8250Å$

The photon having wavelength equal to 8250Å or more than this will not able to overcome the energy gap of silicon.